Pixel detector developments

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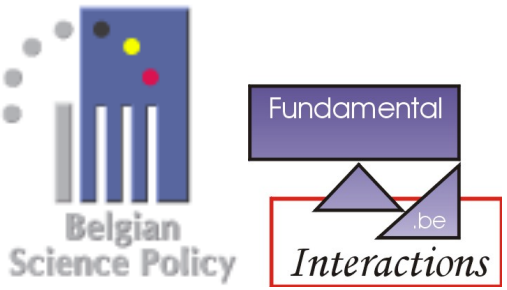

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Introduction

- Particle Physics and Experimental Methods
- Technology Review (HAPSvsMAPS)

SOI pixel project: TRAPPISTe

- Technological Details
- Simulations

NA62: Measurement of rare decay

- Characteristics
- ASIC development for the readout electronics of the GTK

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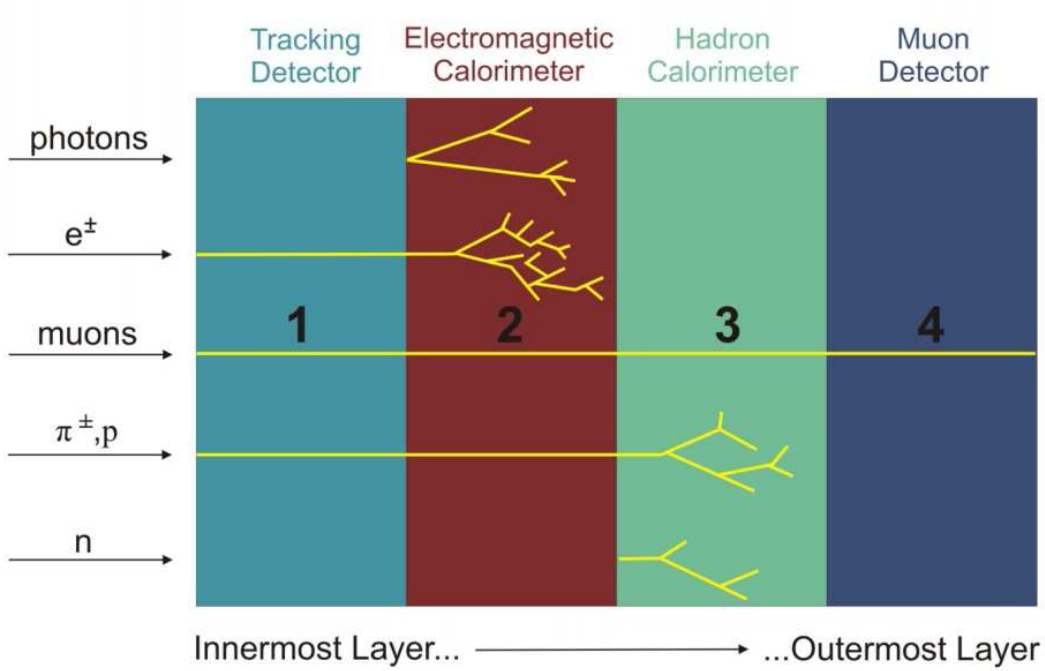
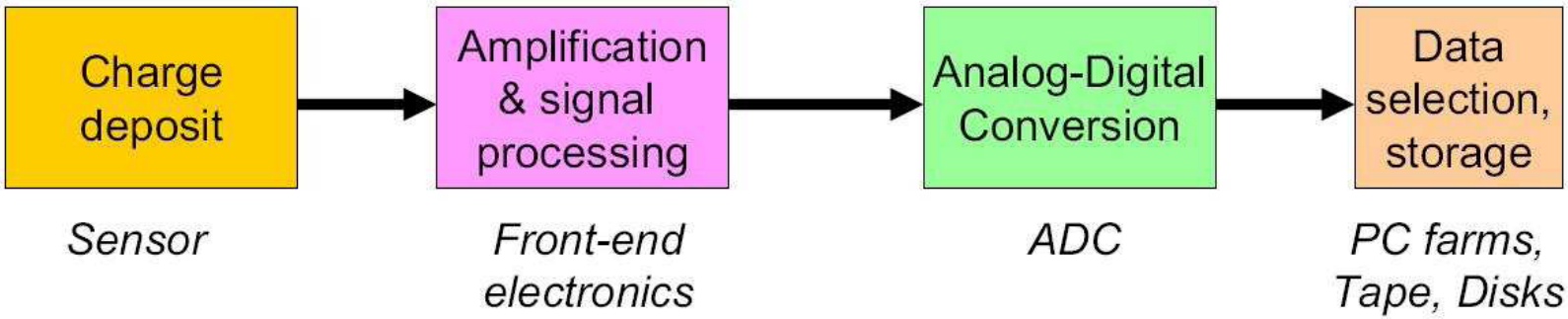
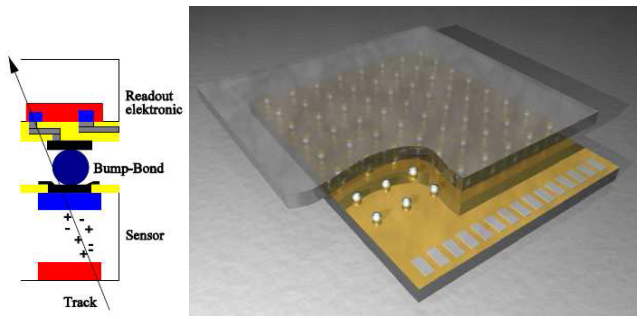

Tracking Detector
Electromagnetic Calorimeter
Hadron Calorimeter
Muon Detector
photons
e±
muons
π±,p
n
1
2
3
4
Innermost Layer...
...Outermost Layer


Charge deposit
Amplification & signal processing
Analog-Digital Conversion
Data selection, storage
Sensor
Front-end electronics
ADC
PC farms, Tape, Disks

HAPS Hybrid Active Pixel Sensor



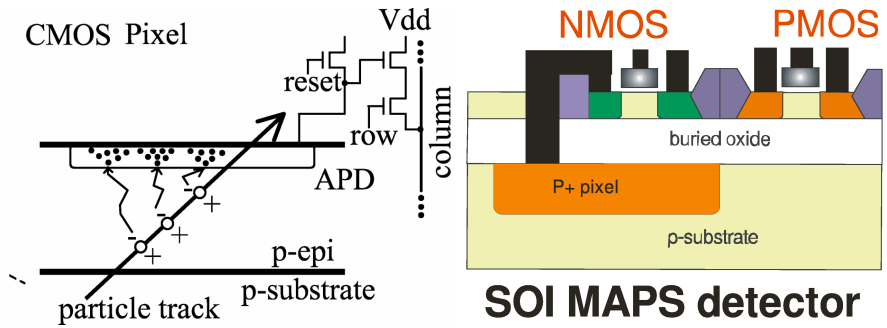
Sensor and FE chip connected through

- Bump bonding, flipchip

Architecture used:

- LHC-collider :ALICE, ATLAS, CMS and LHCb
- Fixed target: NA60, BTev

Monolithic Pixel Detectors



Include amplifying, logic and detecting sensors as one entity

Non-standard CMOS on high resistivity bulk CMOS with epi-layer, CMOS on SOI, Amorphous silicon on standard CMOS ASIC, DEPFET, Deep n-well sensor, 3D packaging

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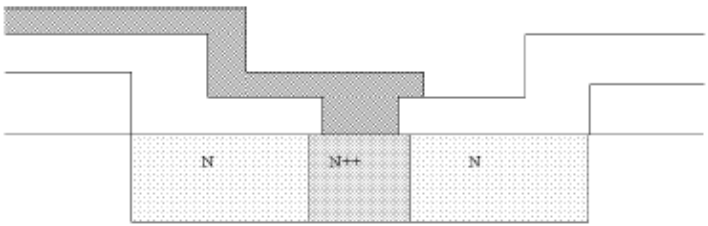
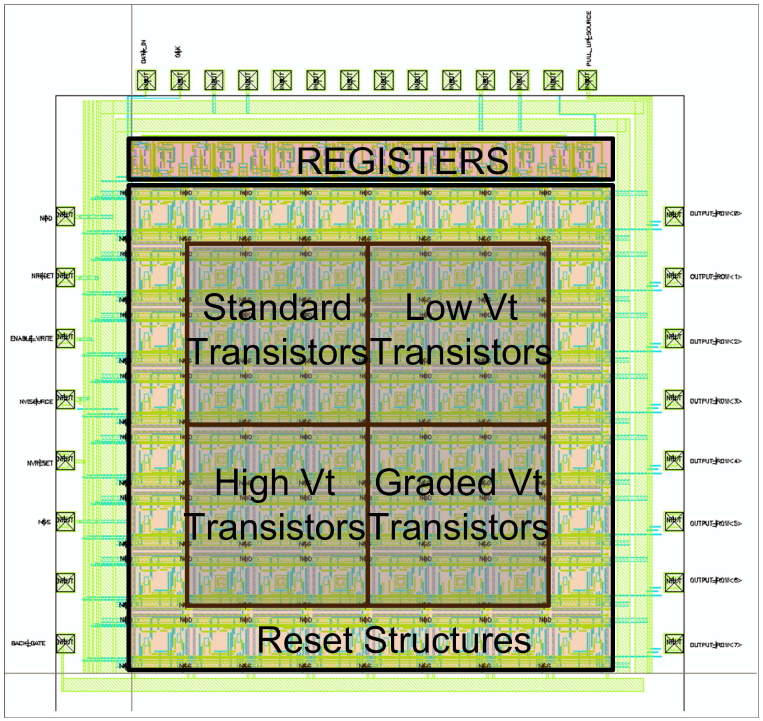
TRAPPISTe-1 (TRAcking Particle for Physics Instrumentation in SOI Technology)

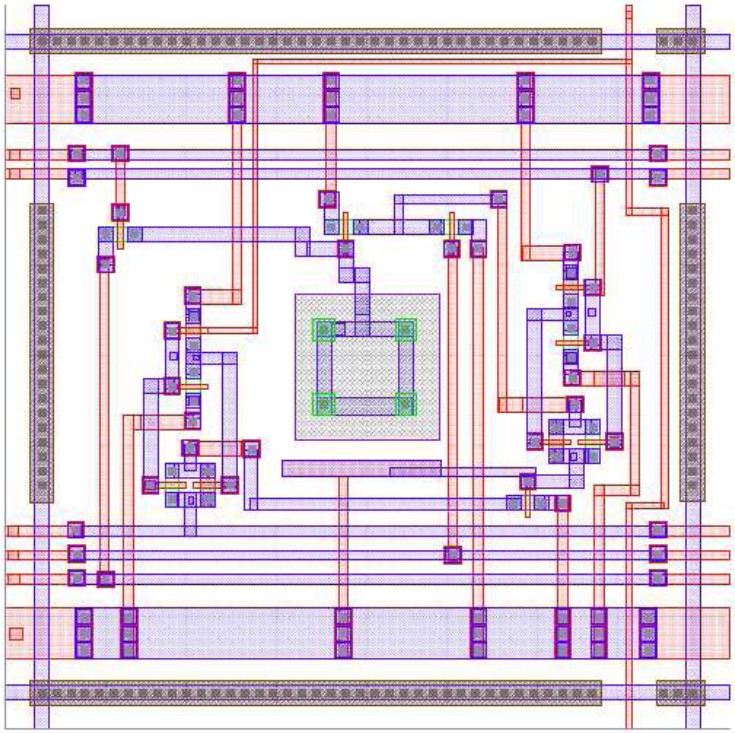
- R&D project for the study of the feasibility to build a Monolithic Active Pixel Sensor (MAPS) with Silicon On Insulator (SOI)
- First prototype has been built with a 2μm technology in SOI production facility in Louvain-la-Neuve



A hole is created in the buried oxide layer to dope the bulk layer P-type bulk with n+ region
Not covered in metal to allow top illumination

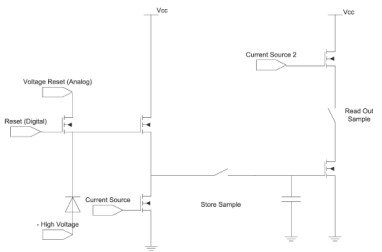


$\text{Area}_{prototype}$=3150×3150μm, with matrix of 8×8 pixels with a size of 300×300μm
An external ring of pixels will be grounded for a better isolation

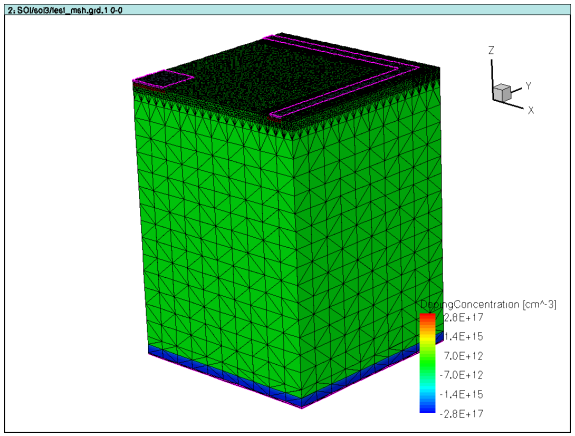


Layout of the detector pixel:

- 10μm width p+-type guard ring
- $60\times60\mu$m centered n-type implant for the detector in the p-type bulk.

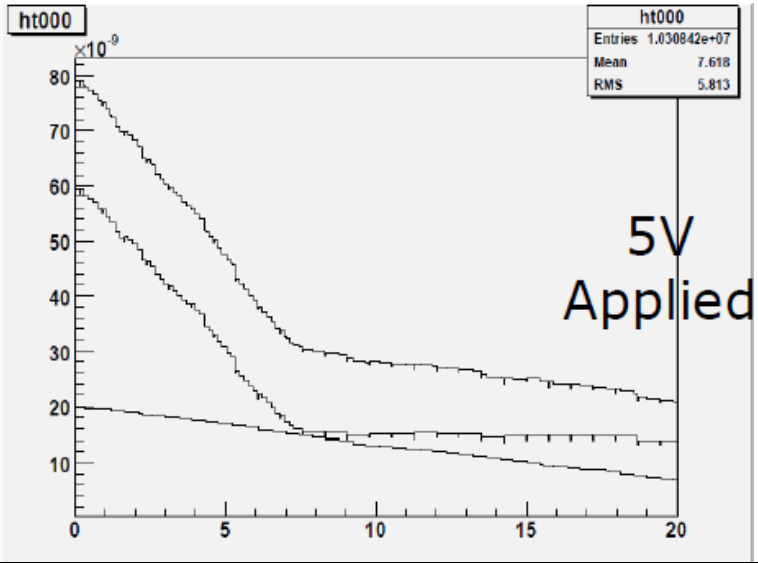


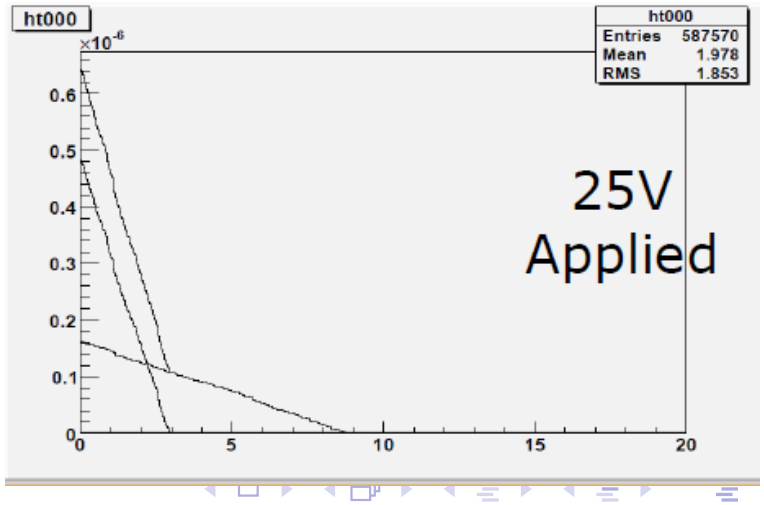
The readout circuitry used is based on the 3-transistor architecture commonly used in MAPS, modified to allow for a pipelined readout

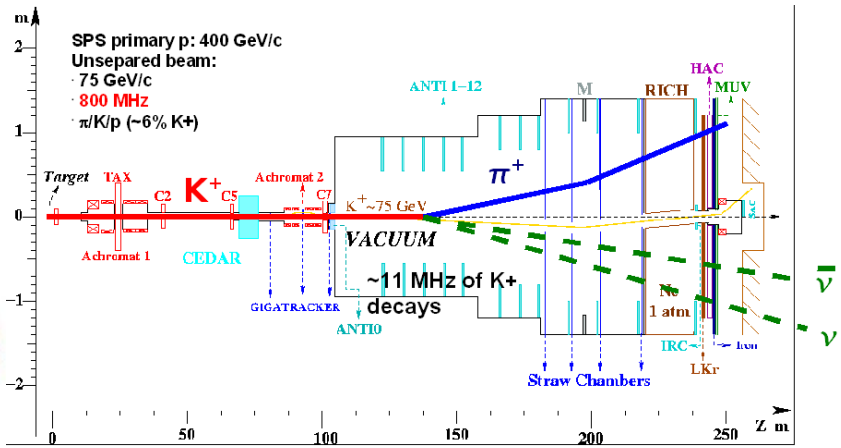


- Depleted region⇒carrier drift
- Non-depleted region⇒carrier diffusion
- Always trapping and recombination

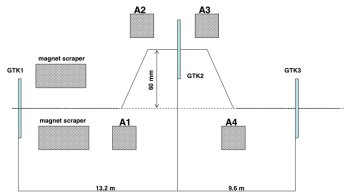
An initial rough estimate of the current signal (thickness of 100μm and a resistivity of 5000Ω/cm.)

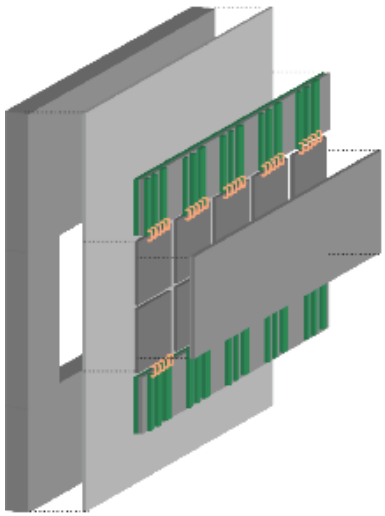






Rare Kaon Decays program at CERN, Measurement of $K^+ \to \pi^+ \nu\nu$





- 3 stations with area $\sim$12 cm^2 each$\rightarrow$ 18000 pixels/station and 2 rows $\times$ 5 columns pixels/station
- Pixel dimensions 300$\times$300μm$\rightarrow$ 1800 pixels/chip
- Radiation levels expected 10^5 Gy and the 1Mev neutron equivalent fluence $\sim 2\times10^{14}$cm^{-2}/year.
- Very low material budget of 0.45 %X$_o$
- Thickness $\rightarrow$ ASIC: 100μm, silicon sensor: 150-200μm
- Analogue FE sensitivity discrimination threshold $\sim$0.5fC.
- Ultra fast analogue FE with t$_{peaking}$ $\sim$3-5ns

Specifications of this detector:

- Time resolution of GTK(rms)150ps, of one station(rms)200ps
- Particle rate/station 800 MHz, Particle rate/chip 130MHz
- Average particle intensity/station 0.5 MHz/mm^2, Peak hit rate of 50 Mhits/cm^2/s
  - **One order of magnitude faster than pixel LHC ASIC**
- Latency $>1\mu$s up to 1ms, with trigger window $\geq$ 10 ns
- Dead time due to read out 1% (2% in beam center)
- Power dissipation per station $\leq$ 2W/cm^2, 32 W
- Operating temperature vacuum $<$ 0 ^{o}C

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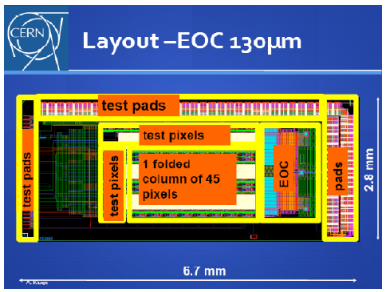
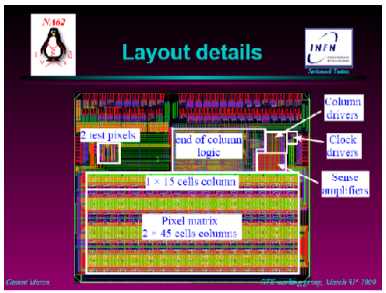
The research for pixel cell design and the readout architectures are following two approaches





- End-of-Column, a classical pixel cell approach (i.e. in ALICE, ATLAS and CMS experiment)
  - Hit signals of TOT discriminator are transmitted via TL
  - Avoids high speed clock in the active pixel array
  - Separation of the EOC digital signals from the analog FE, minimize digital crosstalk
- On pixel TDC
  - More expected crosstalk

Signal shaping of 5 ns peaking time (saturation velocity)
After radiation, charge characteristics degraded
Ballistic effect might affect SNR of channel.

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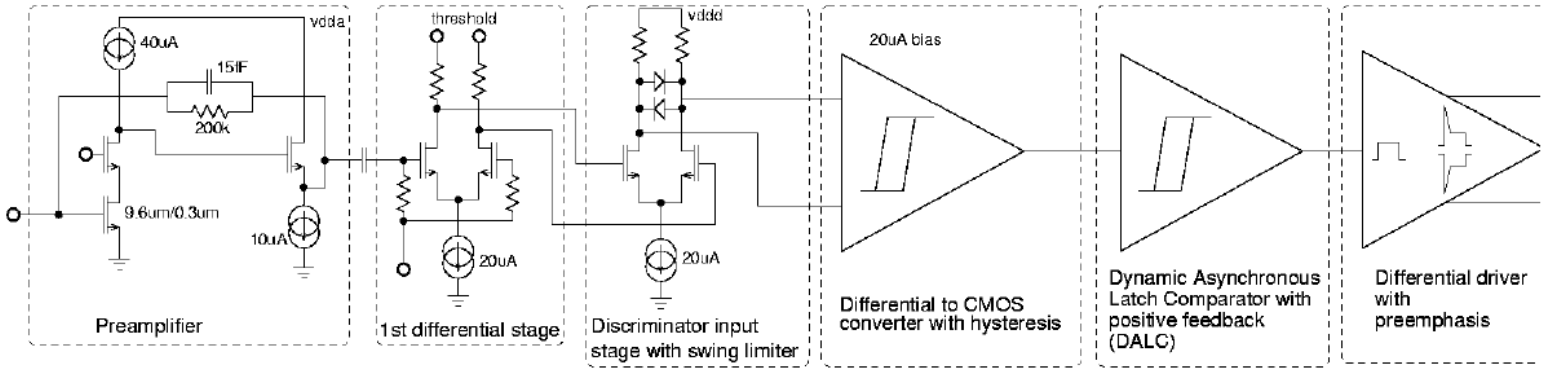
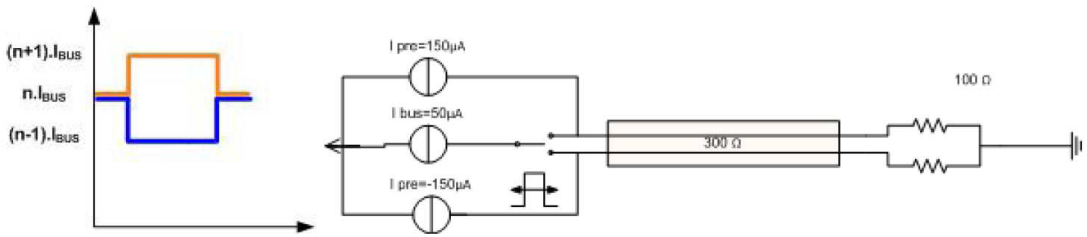


Input stage with cascode-stage (40μA) and a $R_{feedback}$=200kOhm
TL (GHz bandwidth) drived with current mode pre-emphasis
$I_{Bias\ analogue\ pixel\ channel}$=120$\mu$A and $I_{Bias\ TL\ driver}$=80μA
$Gain_{FE\ amplifier}$ $\sim$70mV/fC,
$V_{offset,\ simulated\ mismatch}$ $\sim$6mVrms($\sim$0.1fC signal),
$TW_{comparator}(Q_{threshold}$=0.7fC)=11.5ns between 1 and 4fC signal



Logic level +- 50μA on 250μA bus bias current; right lossy transmission lines driven with pre-emphasis

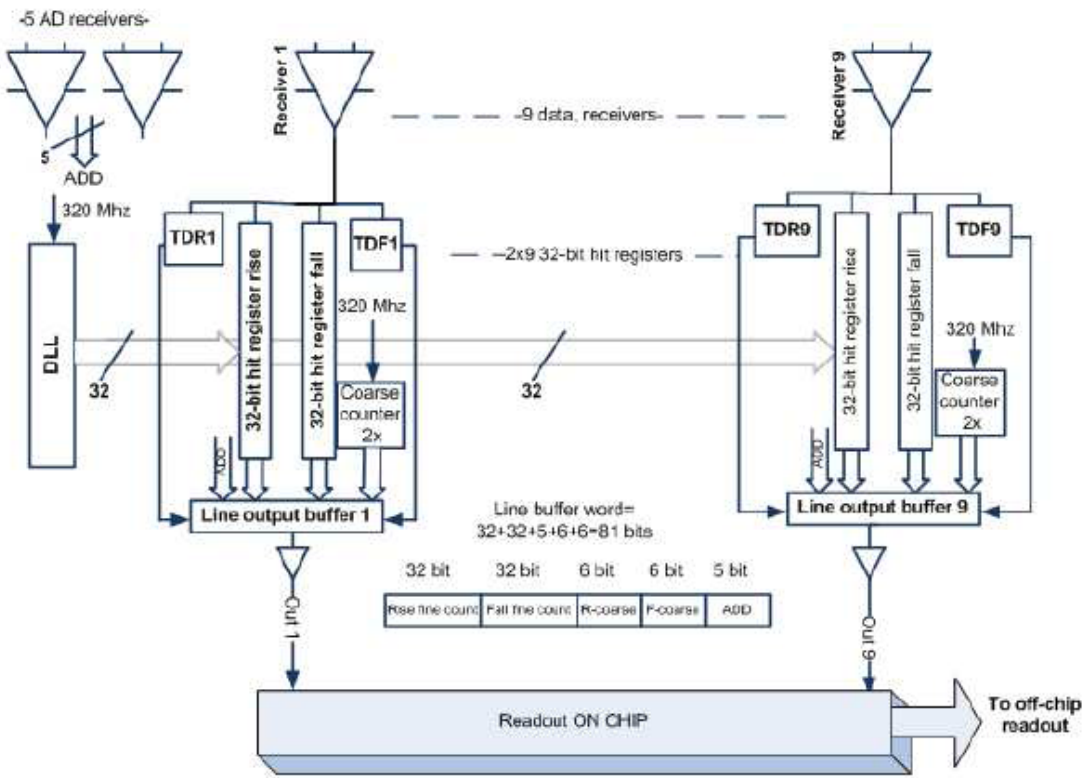
Timing precision of low power signal transmission down to the EOC circuits, with 45 TL(driven in current mode)

- I_{driver} is differential switch with equalization
- $V_{sensing\ at\ far-end}$=0mV for $R_{receiver\ input}$=100Ω
- $R_{line\ for\ 1-45\ pixel\ distance}$=6-30$\Omega$, with $V_{max\ drop}$=3$\times V_{sensing}$

Far end amplitude does not change with receiver distance

Receiver:

- Input stage circuit to sense $I_{differential}$, I_{static} ~250μA
- Broadband differential to single ended amplifier stage
- Generates pulses edges of 50ps to TDC inputs.



End of column circuitry: Receiver bank, TDC bank, Address encoding circuits and Digital logic for processing the hit data ready for transmission off chip.
32-bit DLL and one PLL providing a 320MHz clock signal for the DLL are common to all end of line circuits.

Each TDC presents 2 32-bit hit registers

- Leading and trailing edge of the hit ⇒double time stamping
- Time stamps encoded into 5-bit binary words, stored in a line buffer, serialized and sent off chip