FEC and front-end protection progress

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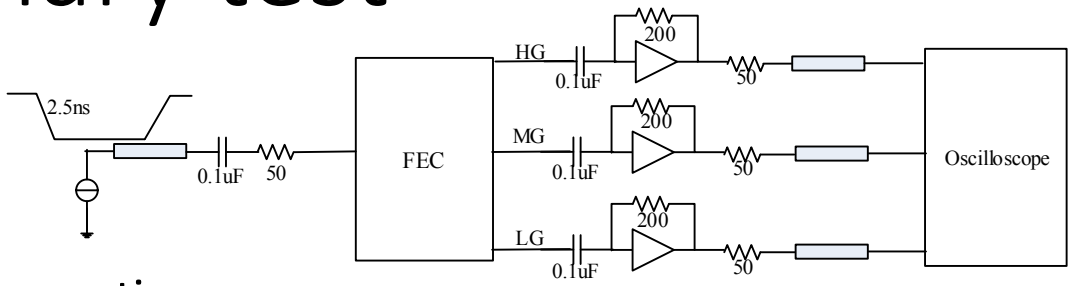
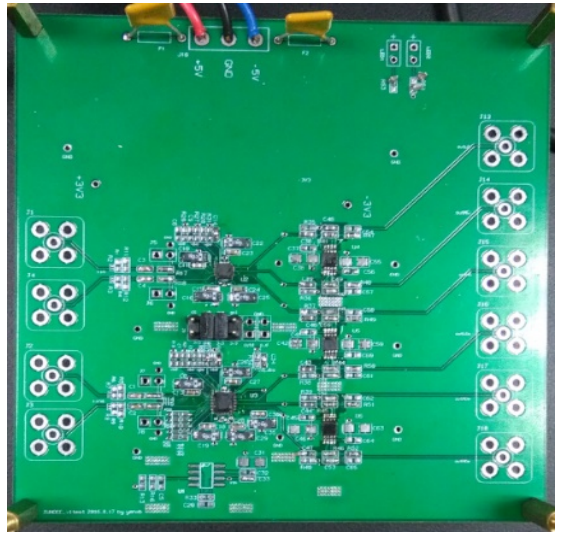
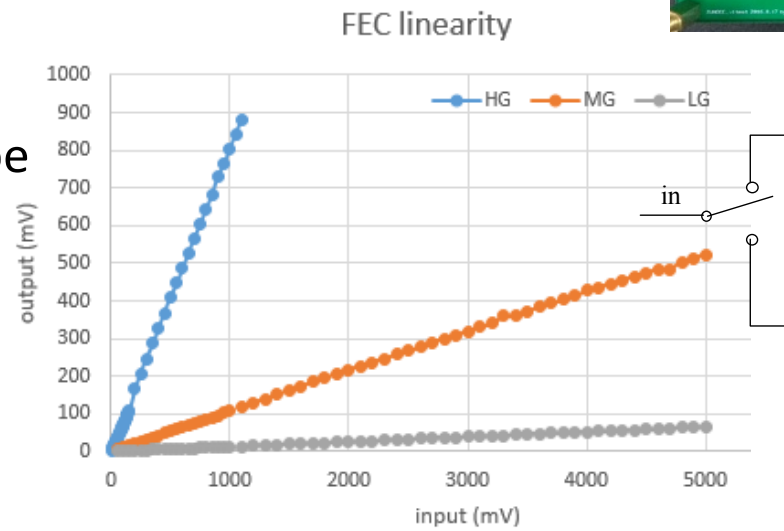
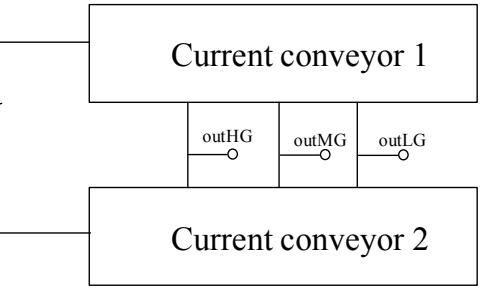
FEC_V1 preliminary test

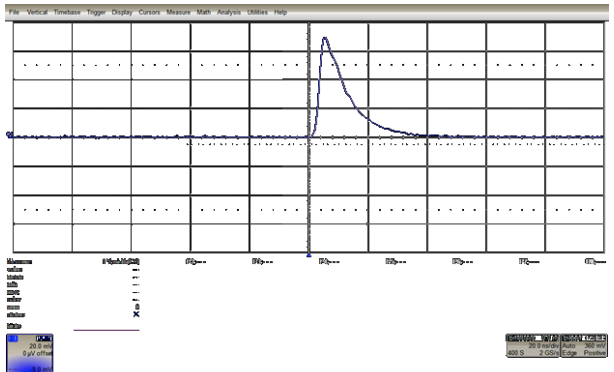


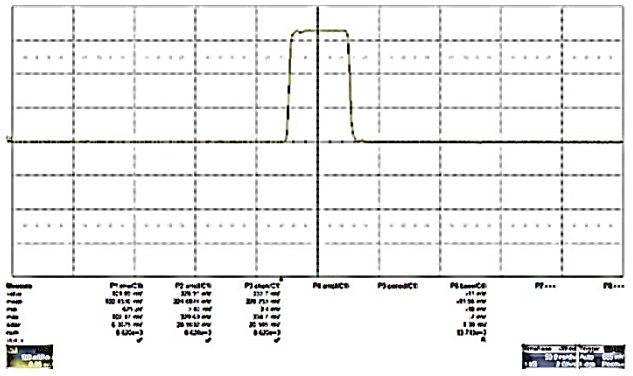


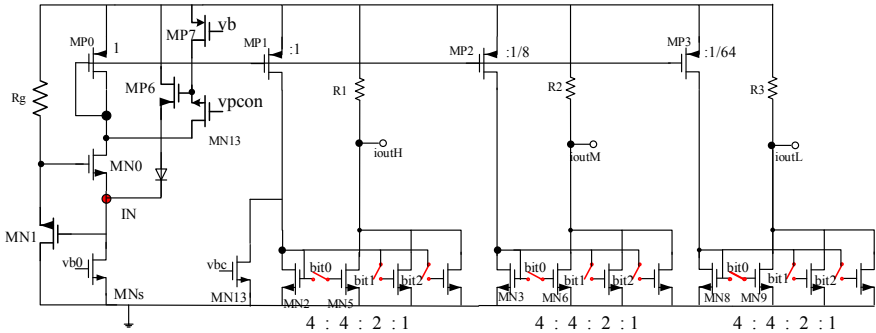
- Redundant design of FEC
- Gain adjustment in case PMT degeneration
- Followed by TIA to increase output current swing
- Input impedance of about 5Ω
- RMS noise equivalent to input 3uA while 120uA for 1 pe
- HG,MG covers whole dynamic range and linearity is acceptable, change LG for HG Redundancy is possible
- Not test to 7.5V input blame to the generator, neither in-chip over current protection
- Difference between not studied carefully





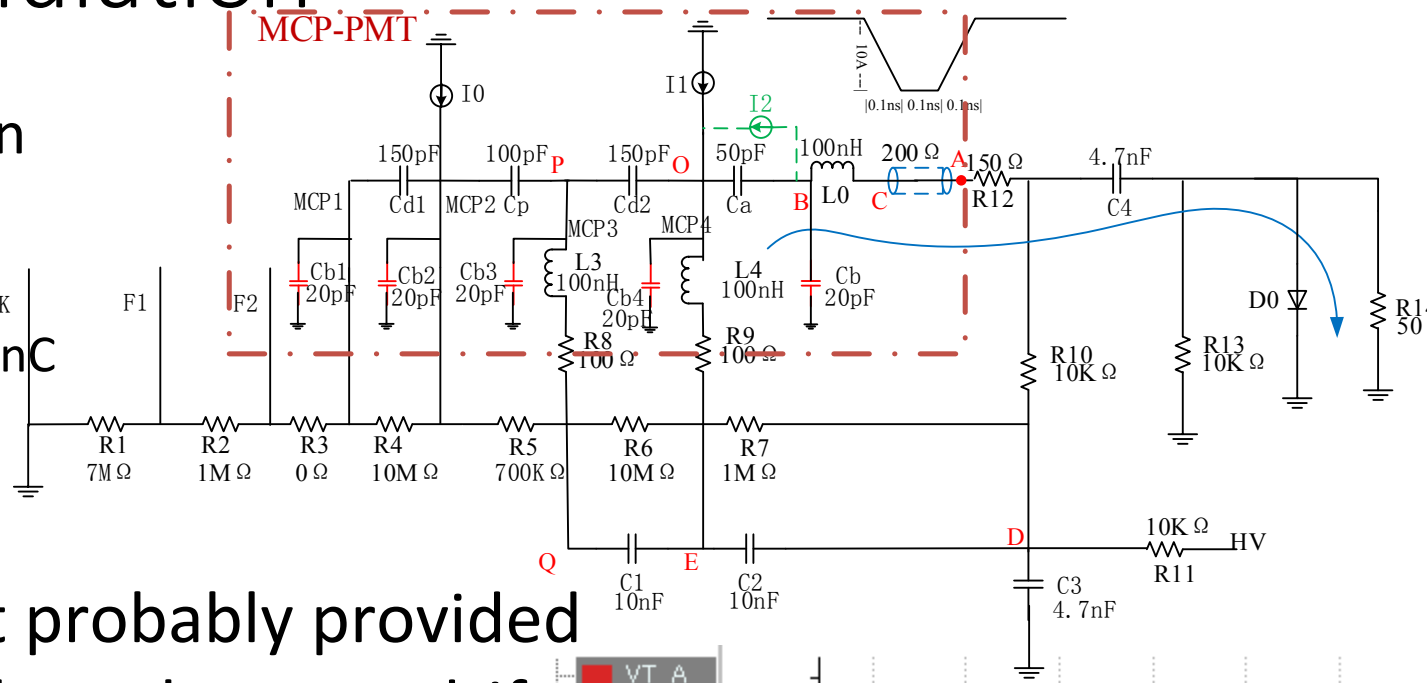




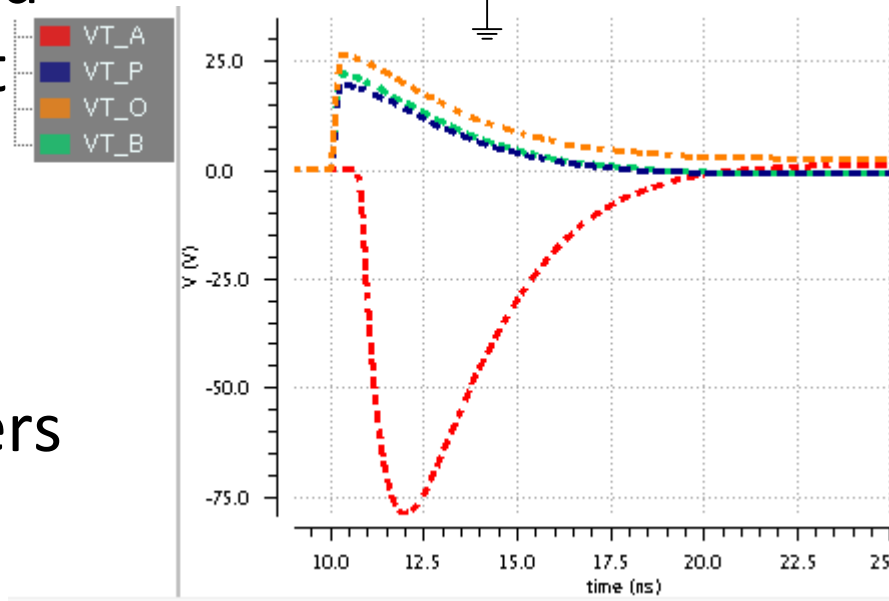


MCP-PMT modeling &simulation

- Hope to find solution of current limitation
- MCP-PMT model：
  - Only last MCP is considered due to the gain
  - MCP presented as Current Source （I_1）of 2nC Charge (1pe*10^7=1.6nC)
  - Parasitic 20pF,100nH at the end of electrode
  - Base of positive HV

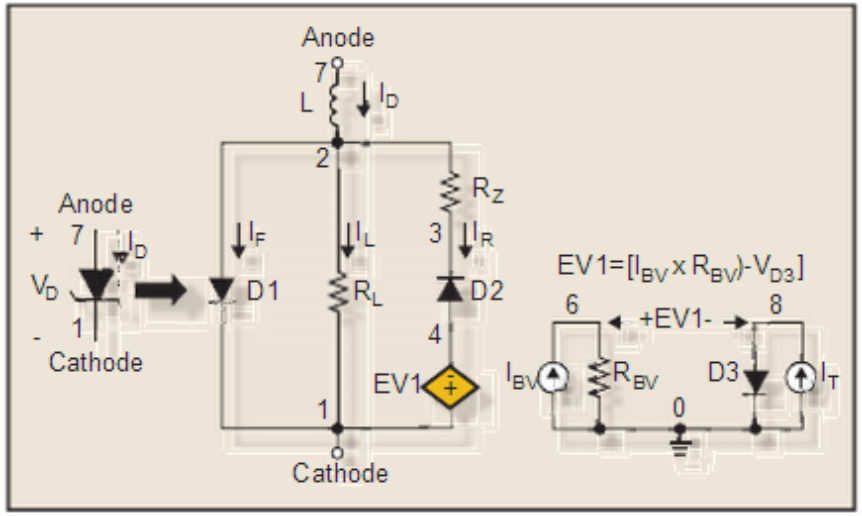


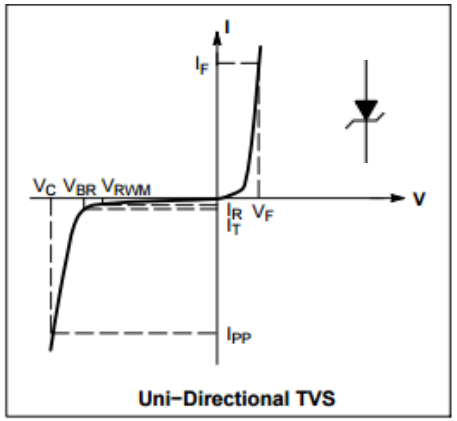
- MCP signal happens, Charge most probably provided by parasitic capacitors very fast, then electrons drift to anode, mainly discharged from output.
- Front edge comes from (L/R), falling edge (CR)
- Potential between electrodes not significant changed, no idea for limiting from divider parameters
- Diode used for protection

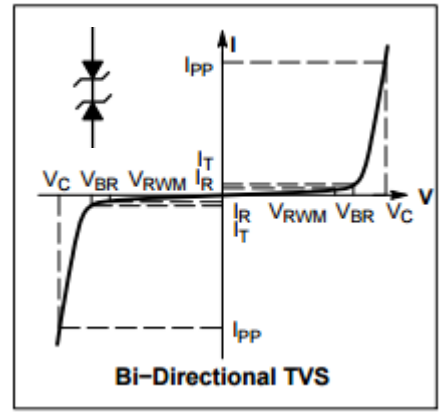


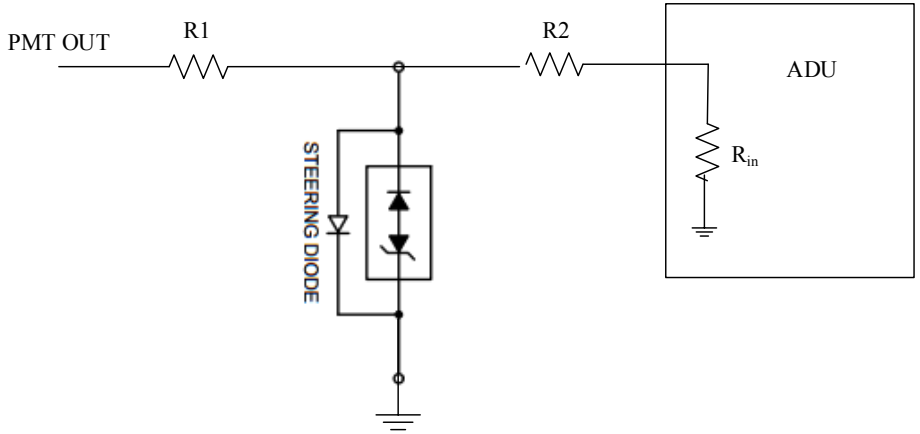
Protection

- TVS (Transient Voltage Suppressor) has very good performance of transient voltage protection
  - $V_{RWM} \approx 0.8 * V_{BR,}$
  - I_{pp} up to several Ampere
  - P_{pk} up to hundreds Walt
  - very fast response time (<1ns)
- Uni-directional TVS has forward voltage around 0.6V
- Bi-Directional protection needed
  - TVS avalanche for negative duration
  - Fast switching steering diode for positive duration
    - I_F up to 200mA,V_R>70V,only consider overshoot
    - Increment of capacitance effect to bandwidth
  - Different clamping voltage for different polarity
  - Reliability not considered carefully
    - Shorted or open when failed?

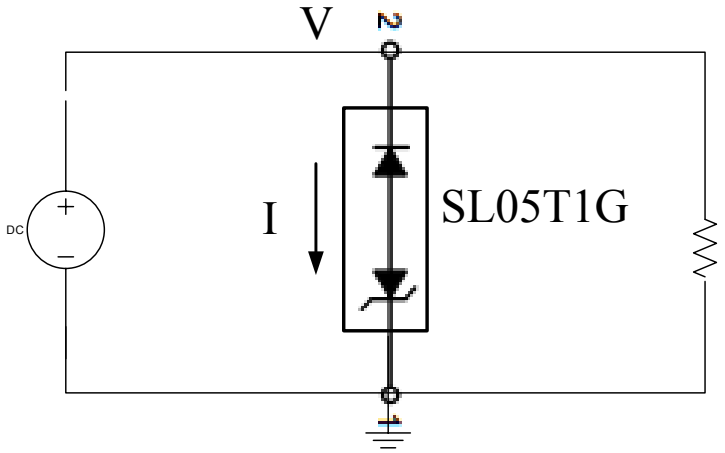






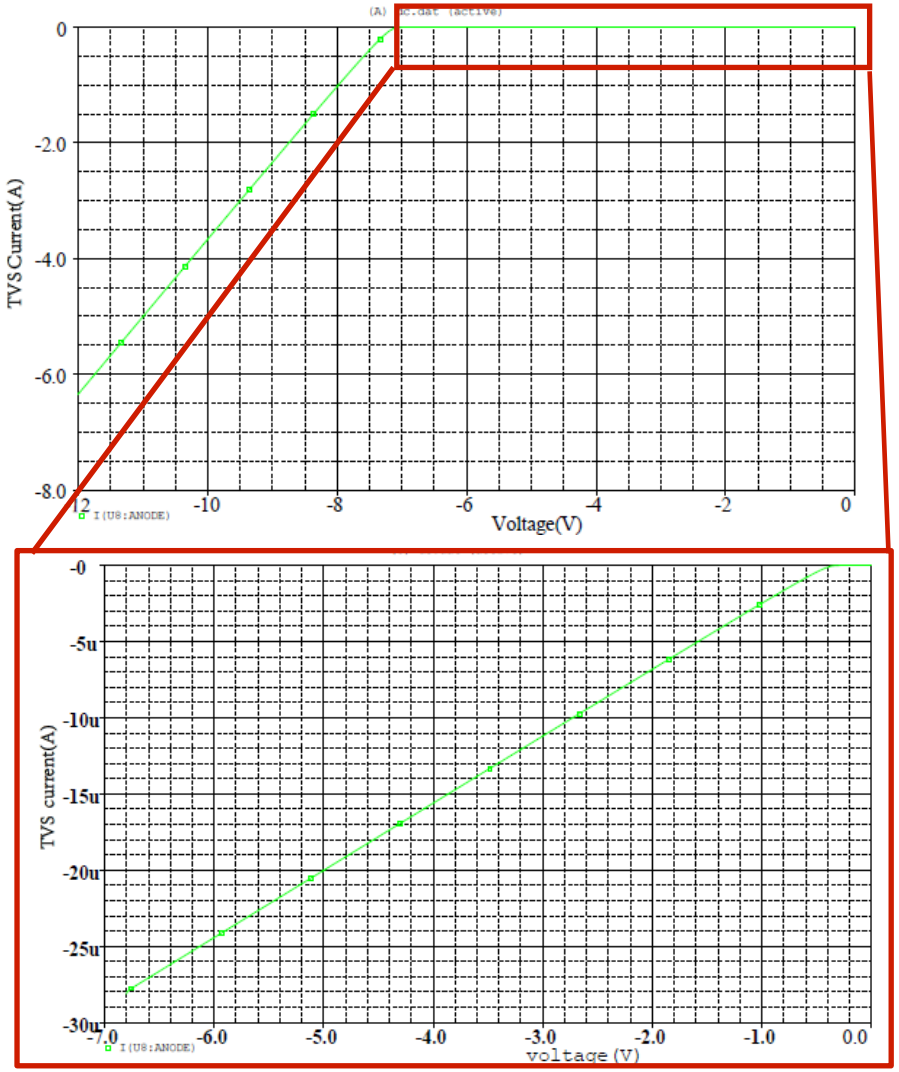


SL05T1G spice model simulation—DC scan

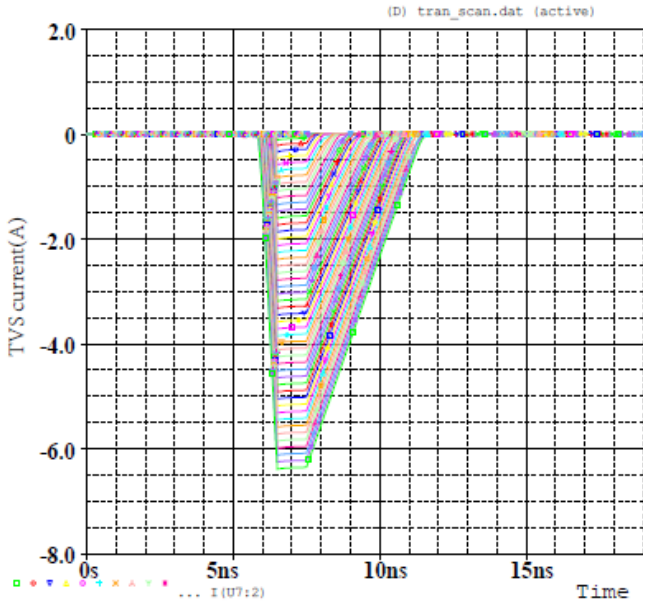


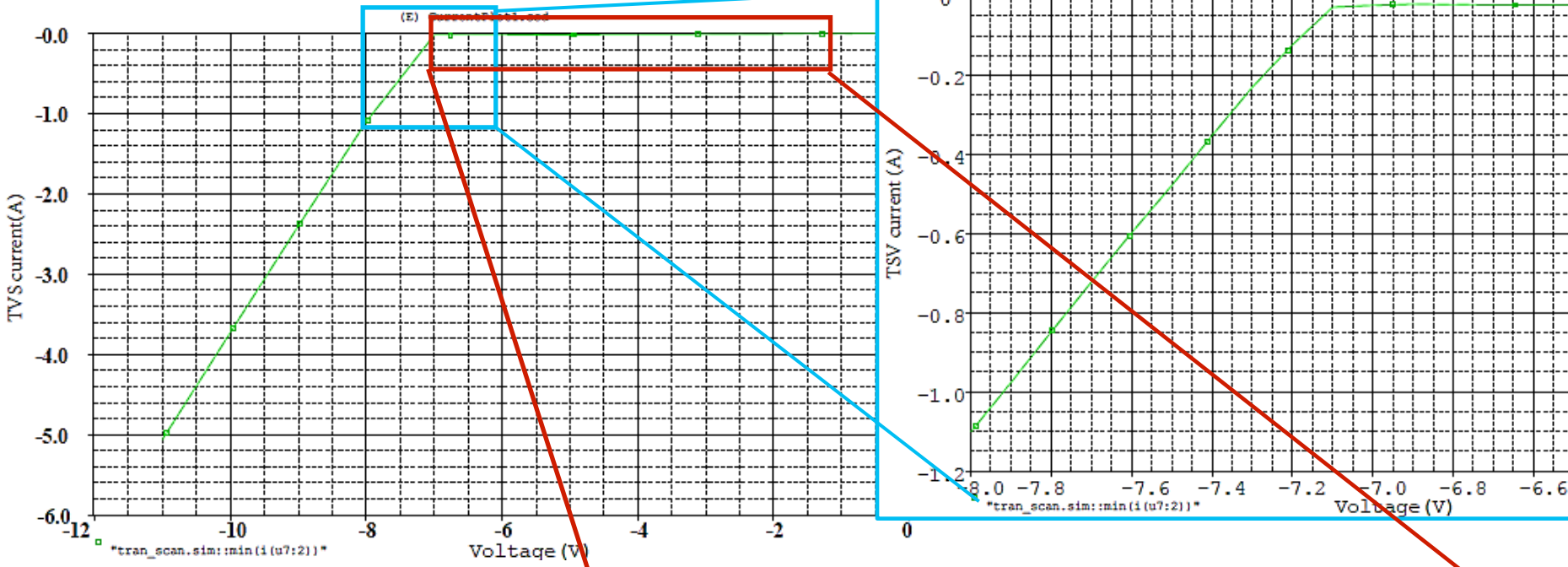
Device	Device Marking	V_{RWM} (V)	I_R @ V_{RWM} (μA)	Breakdown Voltage (Note 4) V_{BR} @ 1 mA (Volts) Min	Breakdown Voltage (Note 4) V_{BR} @ 1 mA (Volts) Max	V_C, Clamping Voltage (Note 5) @ 1 A (V)	V_C, Clamping Voltage (Note 5) @ 5 A (V)	Max I_{PP} (A)	Capacitance @ V_R = 0 V, 1 MHz (pF) Typ	Capacitance @ V_R = 0 V, 1 MHz (pF) Max
SL05	L05	5.0	20	6.0	8.0	9.8	11	17	3.5	5.0

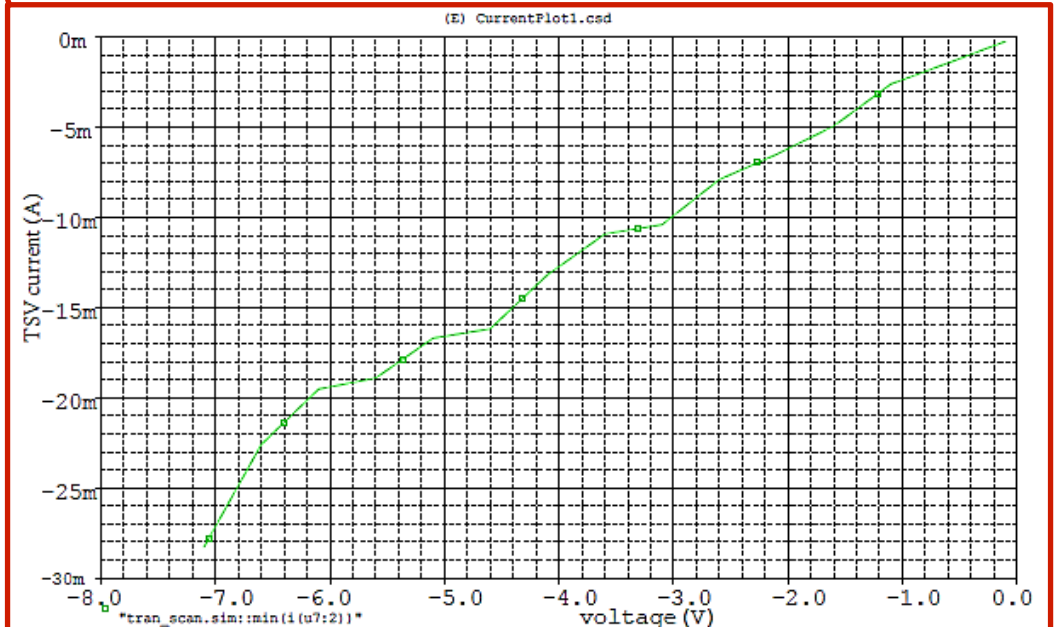
- Reverse leakage current is small, I_R=20uA@5V
- V_{BR}=7V @ I_{test}=1mA
- Vc=8V@ I_{test}=1A;
- Vc=11V@I_{test}=5A



SL05T1G simulation--Transient response







- Input : Tr=1.5ns, T_f=10ns,w=1ns
- Transient reverse performance is similar as DC reverse biased
  - V_{BRt}=7V@I_{testt}=28mA, I_{testt}=0.5A @V_{ct}=7.5V
  - Before avalanche, equivalent to a capacitor of about 5pF(or Z=300)

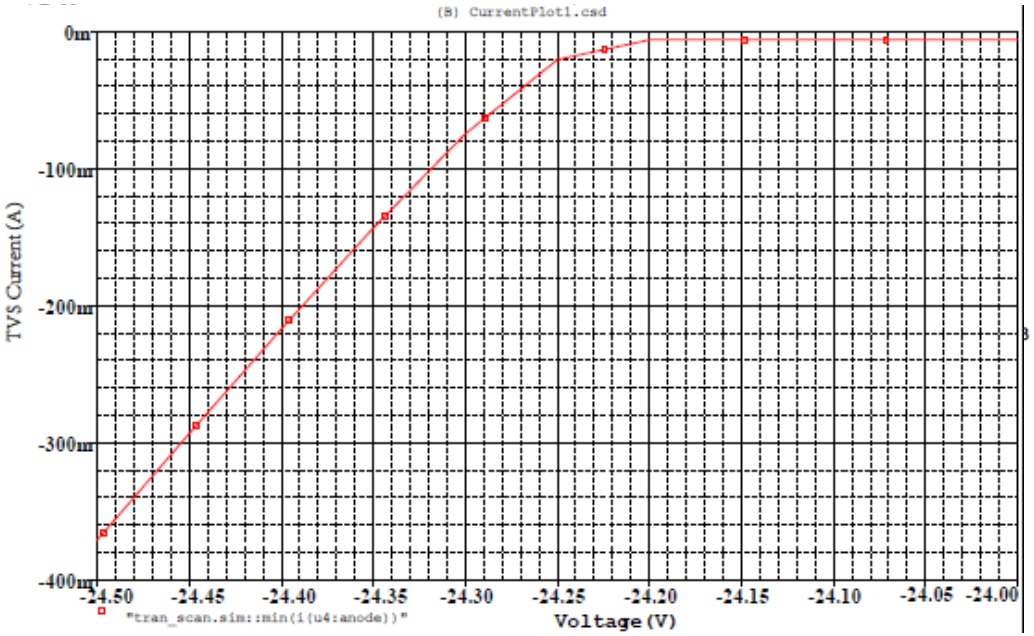
ESD7361HT1G simulation—transient response

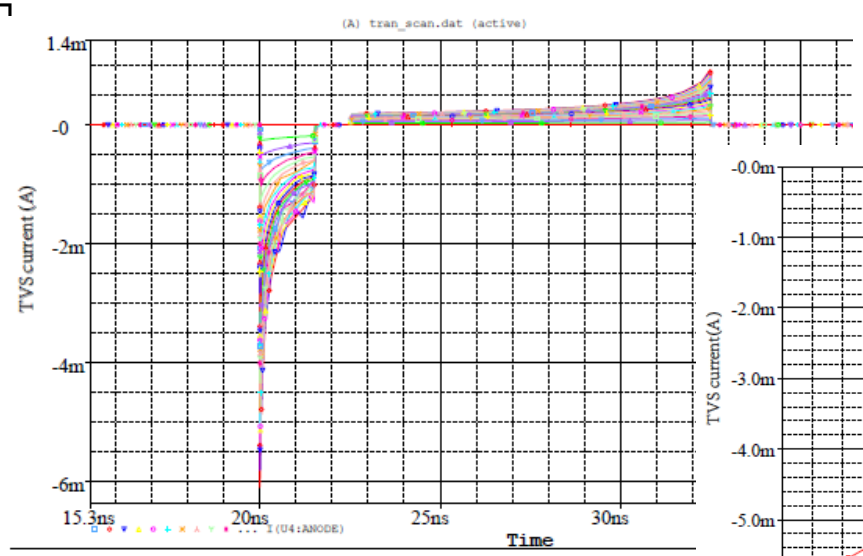
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

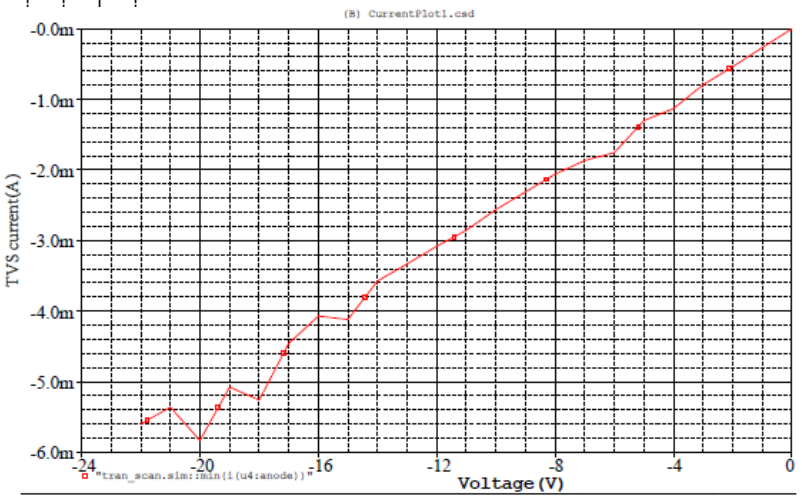
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}			5	16	V
Breakdown Voltage	V_{BR}	I_T = 1 mA; pin 1 to pin 2	16.5			V
Reverse Leakage Current	I_R	V_{RWM} = 5.0 V		<1	1000	nA
Clamping Voltage (Note 2)	V_C	I_{PP} = 8 A		31		V
Clamping Voltage (Note 2)	V_C	I_{PP} = 16 A		34		V
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz V_R = 0 V, f < 1 GHz			0.55 0.55	pF
Dynamic Resistance	R_{DYN}	TLP Pulse		0.735		Ω
Insertion Loss		f = 1 MHz f = 5 GHz		0.01 2		dB

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. For test procedure see Figures 9 and 10 and application note AND8307/D.
2. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
   TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 4 ns, averaging window; t_1 = 30 ns to t_2 = 60 ns.







- Transient performance is similar as DC reverse biased
  - Before avalanche equivalent to a capacitor of around 0.5 pF(or Z=4K), higher Z than SL05, less signal loss
  - V_{BRt}=24.2V I_{testt}=6mA, I_{testt}=0.4A @ V_{ct}=24.5V while having mini V_{BR}=16.5V
  - Without typical V_{BR}, not know variation, how to select?

conclusion

- FEC preliminary result meets the basic requirement, test not finished----New package, and improvement
- MCP-PMT model need to be verified by experiment and refinement
- TVS with Higher V_{BR} is better for protection, need testing and selecting
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