PMT, Base and Receiver Interface

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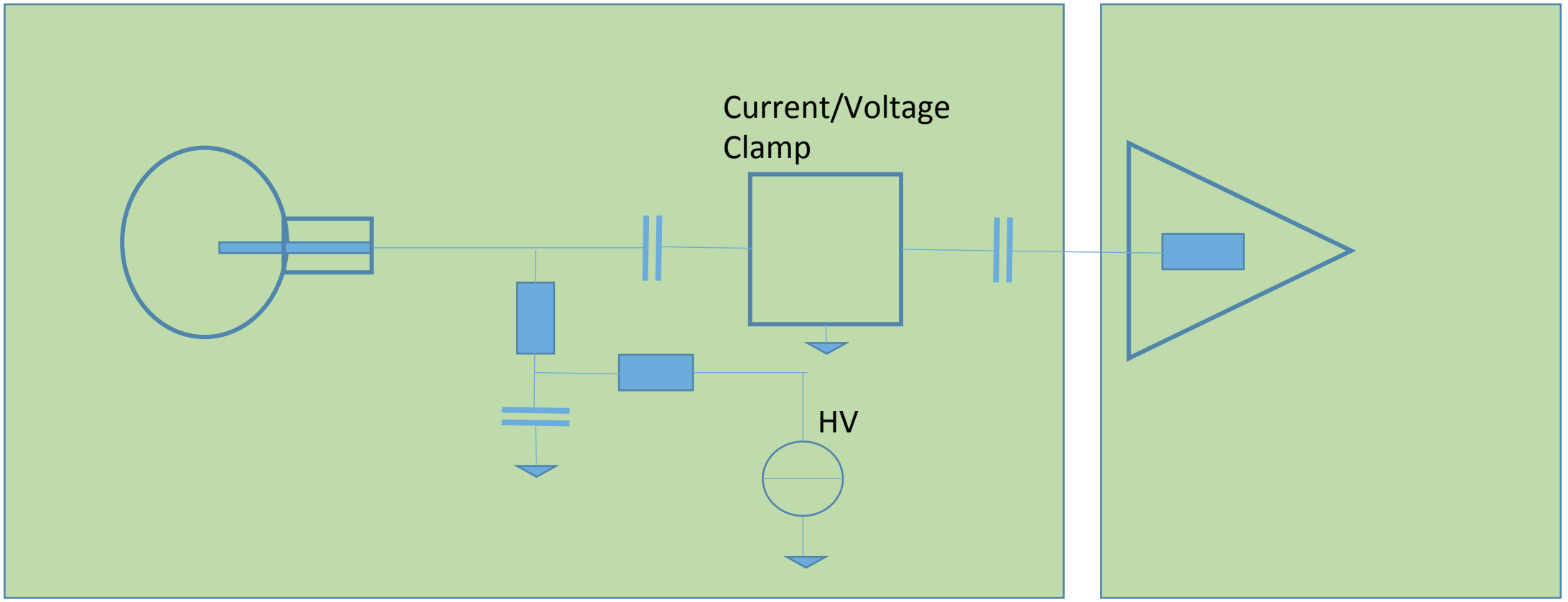
Protection

- There are three kind of large signals:
- Spark:
  - One of the high-voltage elements could have a discharge, worst case the signal point could drop by 2kV.
  - The signal-voltage would follow
  - With a good base design, spark should be very seldom, less than 1/Year?
  - High Bandwidth?
  - More resistors in serial to reduce the voltage across one element, that is the current design.
- Large signals from the PMT
  - The linearity of the Receiver is up to 1000 pe, setting the maximum input current at ca. 150mA
  - Measurements show currents up to 600mA. This can happen frequently (muons) with MCP-PMT. It must be simulated or measured if the signal bandwidth is lower (Time of flight variation)
- Ramp up of the HV
  - How fast will the HV ramp up?

Discussion on PMT base ↔ ADU interface

- Signal definition:
  - How much charge can the PMT give?
    - Capacitance of the PMT structure
    - Voltage over the capacitance?
  - PMT output measured:
    - Hamamatsu: 0~-8V with 1% overshoot on 50ohm
    - MCP PMT: 0~-32V with 1% overshoot on 50ohm
- What determines the bandwidth of large signals?
  - Variation of time of flight in the PMT
- What is the Bandwidth of the small signals
  - Measurements show 1.2ns,
  - Hamamatsu should be 2ns, which is the goal in order to get 2 samples on a rising edge

System Overview Discussion



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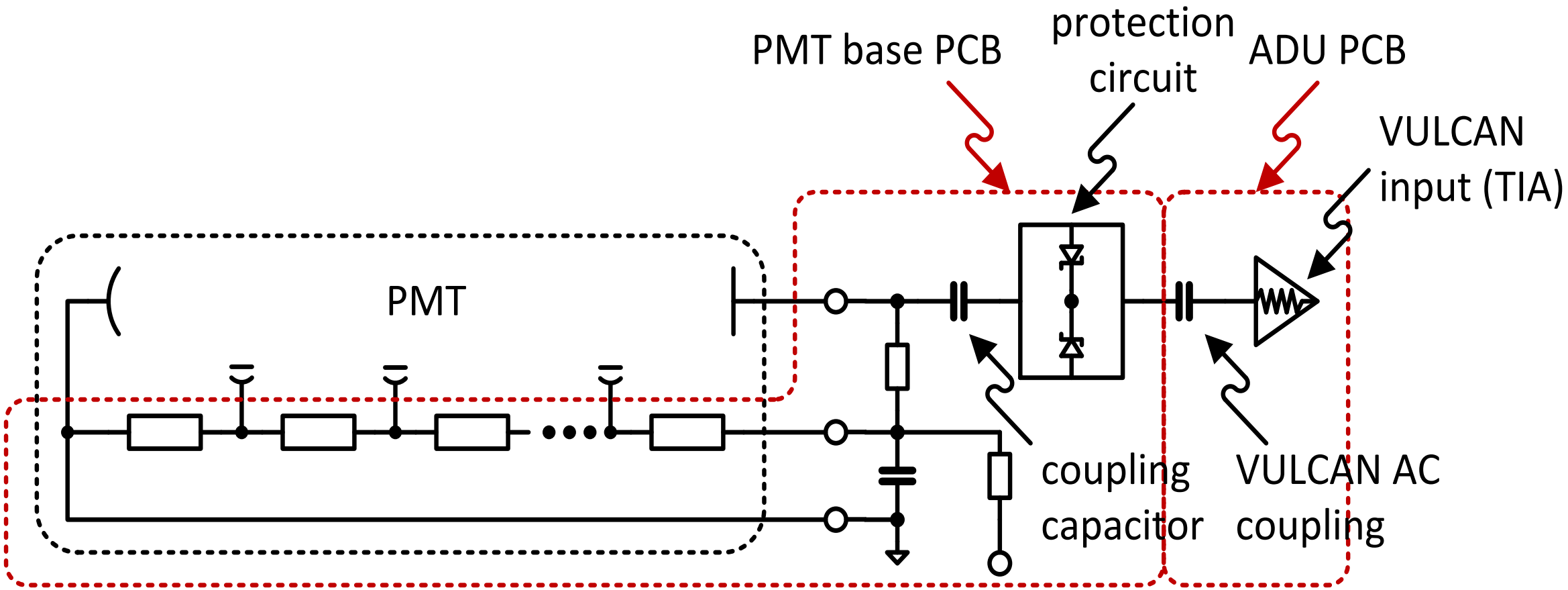

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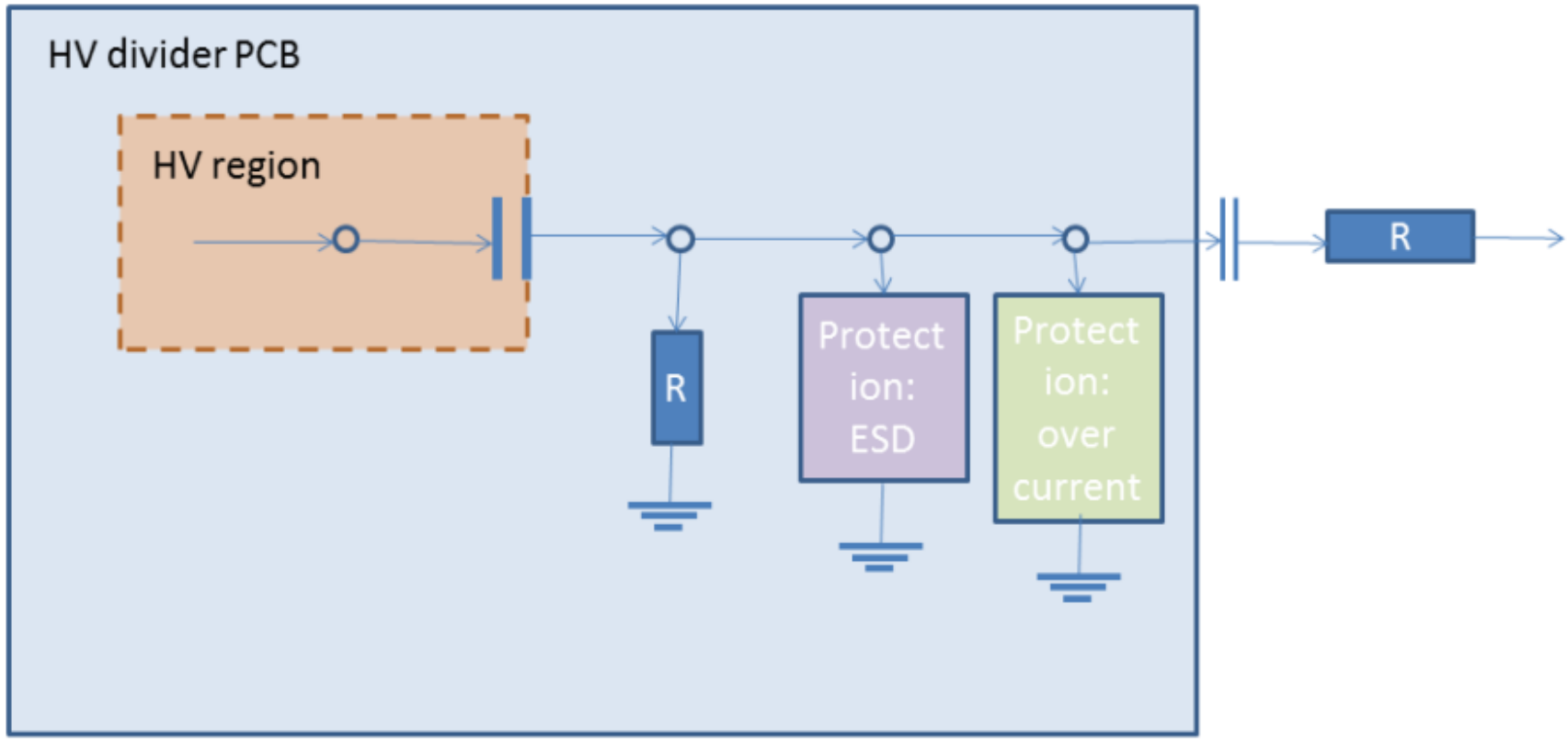

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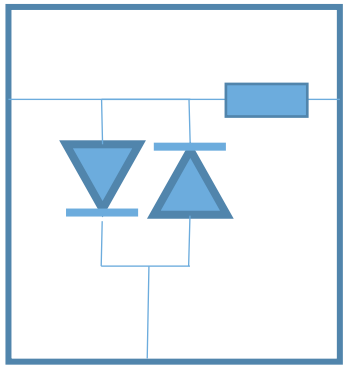
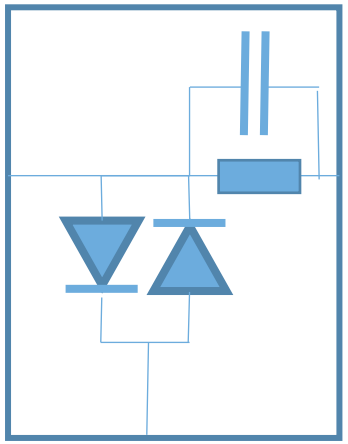
How does the clamp look like?



TVS with shunt resistor



TVS with shunt resistor and highpass

- Approaches for protection
  - PSR: Pressure sensitive resistance
  - ESD: Electrostatic discharge
  - TVS: Transient voltage suppression
  - Arrester: https://de.tdk.eu/inf/100/ds/S30-A75X-X1023T203.pdf

- Questions:
  - Reliability?
  - What is the behavior if broken? (open/close)
  - Highvoltage behavior?
  - Resistorvalue?
  - Influence on Noise and OSC?
  - Signalshaping needs testing!
  - Capacitance should be < 5pF
  - Response time?
  - Variation of clamp voltages?

Open tasks

- Characterize the MCP-PMT in more detail. Probably it is a good idea to create a model of the MCP-PMT.
- Calculate total charge, a PMT may deliver.
- Do we need negative supply?
- Protection range will vary, which is the minimum range in relation to the needed linearity? (0-7.5 V at 50 Ohm to be discussed.)
- How much variation does each protection has?
- What is the time behaviour of the clamp and ESD? What pulses can the chip survive?
- Diodes would show better reliability, but will fail as a short.
- The value of the resistor is depending on the knee-voltage of the clamp (now the voltage is 7.5 – 8V)
- What is the parameter of the already designed protection of the chip (ESD)?
- Reliability of the Protection itself? (0.25% in 6 Years? Since the PMT is 0.5% in 6Years, does it has to be better? tbd)

Ideas for PMT signal limitation and protection

- Bird view of current protection ideas
  - ESD: HDM, MM to +/-4000V?
  - Limitation of output up limit to -160mA? And maximum current <-640mA?
  - How about overshoot?
- Protection design of current electronics
  - Valid range: 0~-160mA?
    - TIA: 0~-19.2mA. How about overshoot? Overshoot input is highohmic (0-3.3 V)
    - If the input current exceeds 20mA, the ESD protection will take the current, but not above 160mA.
  - What kind of protection already realized on electronics input? And parameters?
- Requirements to DC power from protection
  - If diode option: need ~7.3 V stable DC power and up to 640mA current pulse maximum? Must be buffered by capacitances.
  - Any voltage between 1.79- 20V is possible, what are the ripple requirements?
  - How about the reliability of the regulator, is it part of the base?
- Requirements to grounding
  - Need the grounding can handle 640mA current for over current and several 10s A for ESD?
- Possible options for ESD and over current, and how to avoid short if broken.

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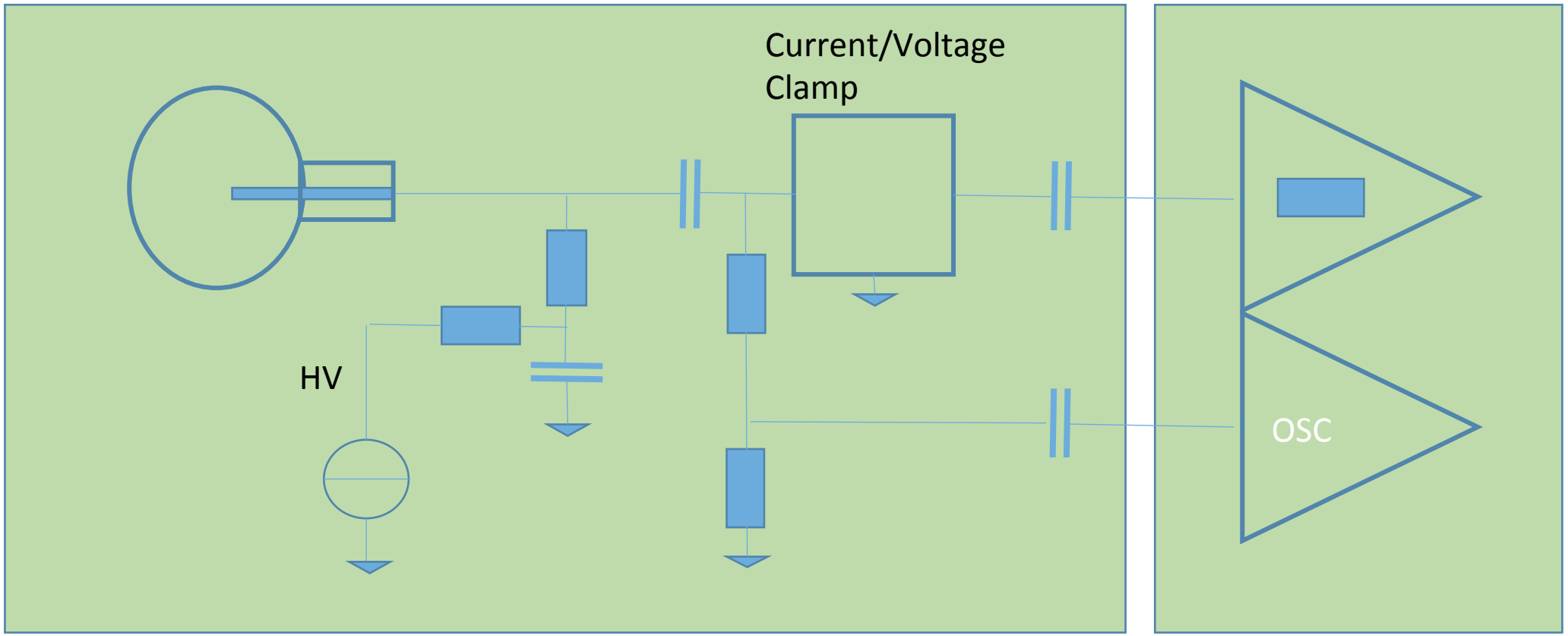
And comments from Robens and Steinmann

Summary of Action items:

- Reliability of arresters and TVA
- Simulation of the OSC with a train of pulses
- Design of OSC input
- Build a model of the PMT
- Size of the resistor in the clamp, in serial to the TIA input
- Calculate the resistance in the clamp and check noise behavior
- Check the ADC ranges: can the middle ADC range be changed to have a lower ADC range reference to catch the overshoot signal?

Discussion of the Design of OSC input



Build in selftest elektronics

Vulcan can be programed to send a test signal into the inputnode of the signal:

The DAC specification is:

Fclock=250MHz

Vsignal= 0,1V – 0,9V

The signal can be programmed with 256 * 8 bit words