Progress of the Tsinghua ADC and Packaging

Wei W., Li F.L., Yan X.B., Hu J.

Institute of High Energy Physics, CAS
State Key Laboratory of Particle Detection and Electronics
On behalf of Fule's team

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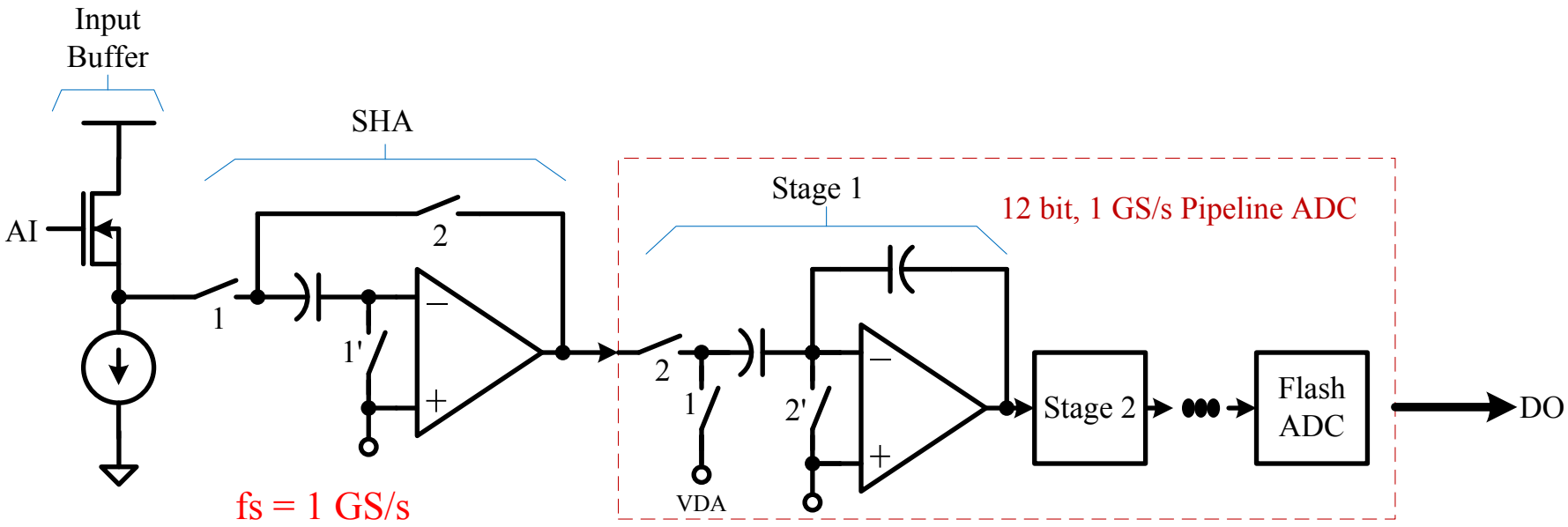
Outline

- **Progress of the Tsinghua ADC**
  - **General overview**
  - **Test results of the 2nd version**
  - **Improvement of the 3rd version**
- **Status of the advanced packaging R&D**
  - **General ideas**
- **Plans**

General overview of the Tsinghua ADC

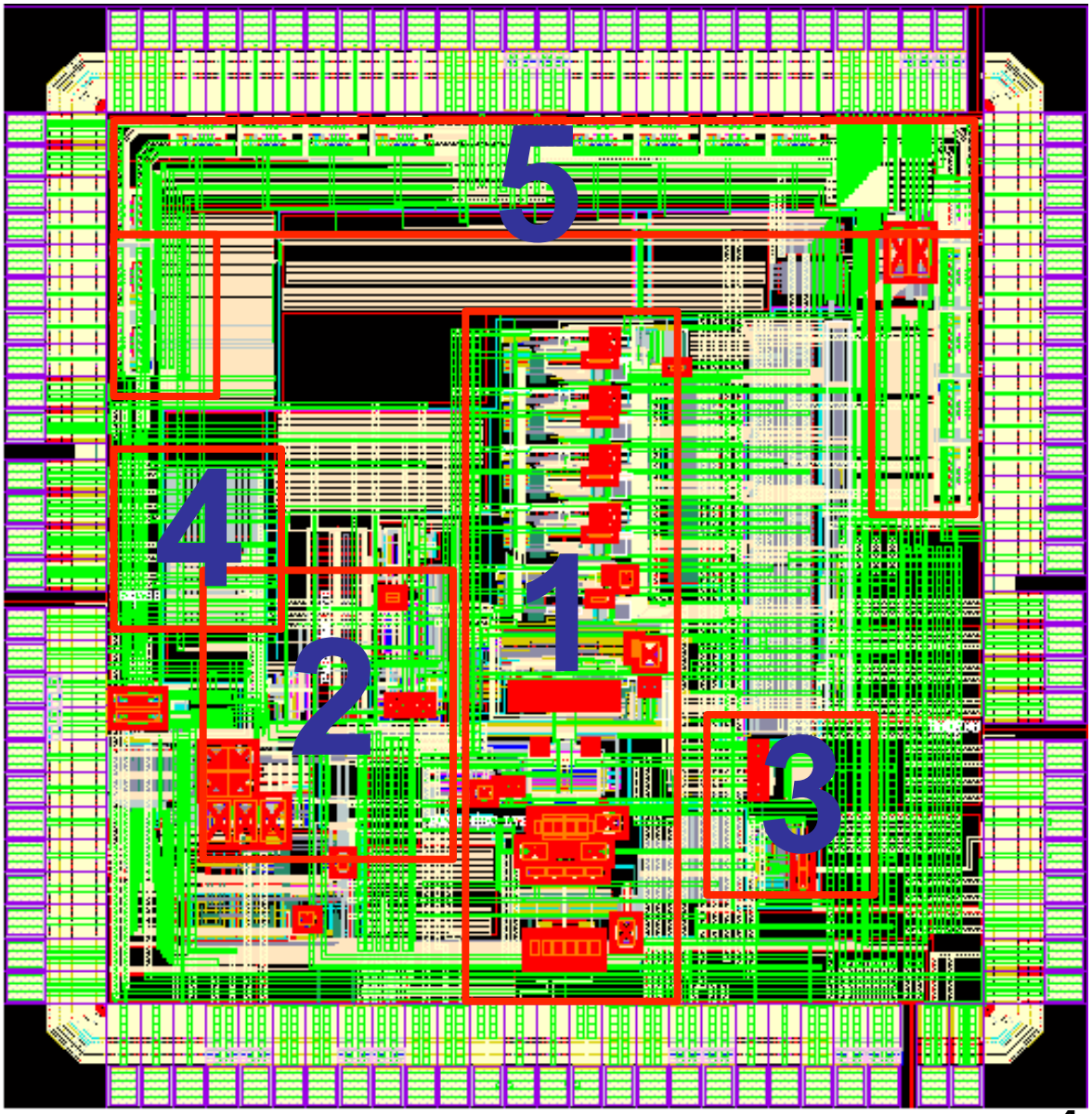


- **Single channel realization for the sampling rate up to 1 GS/s, no time-interleaving calibration required**
- **On-chip reference generator**
- **LVDS output @ 1 GS/s**

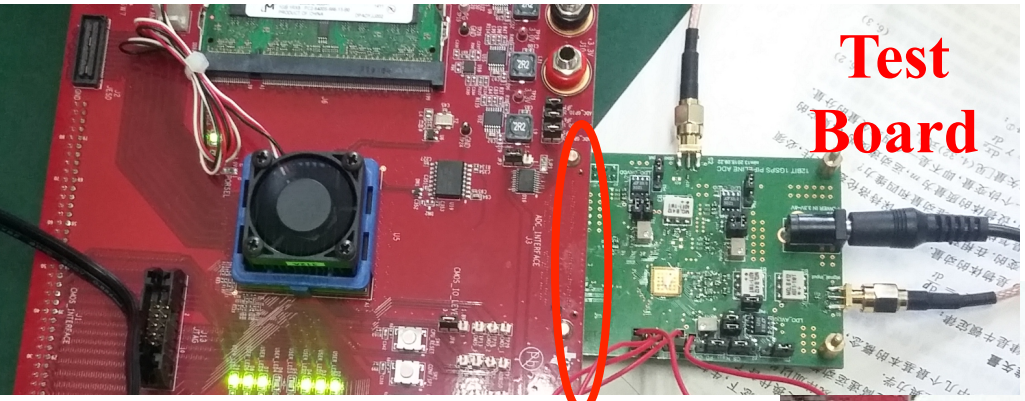
Chip Layout

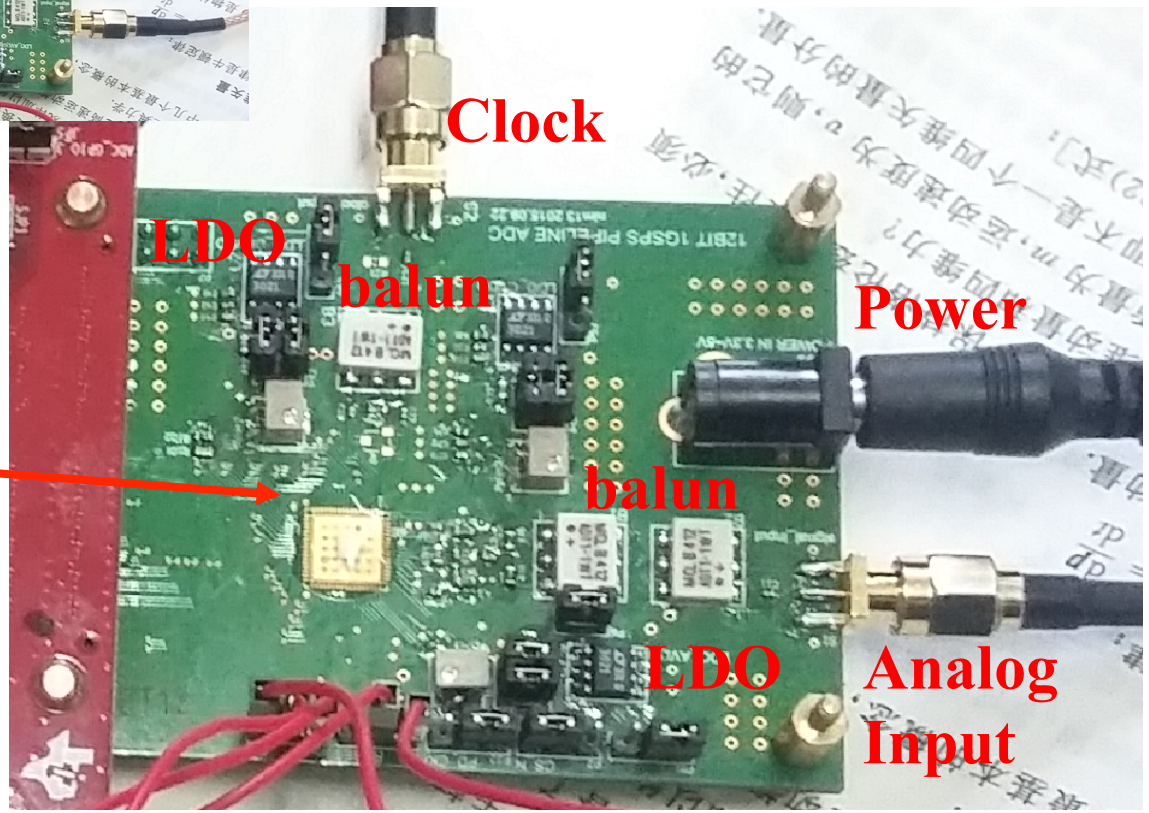
1. AD_CORE
2. Bandgap,
   Reference buffer
3. Clock amplifier
   and generator
4. SPI
5. LVDS buffer, LDO

- Total chip size:
  2mm*2mm
- The 2nd version
  taped out on 23
  Feb. 2016



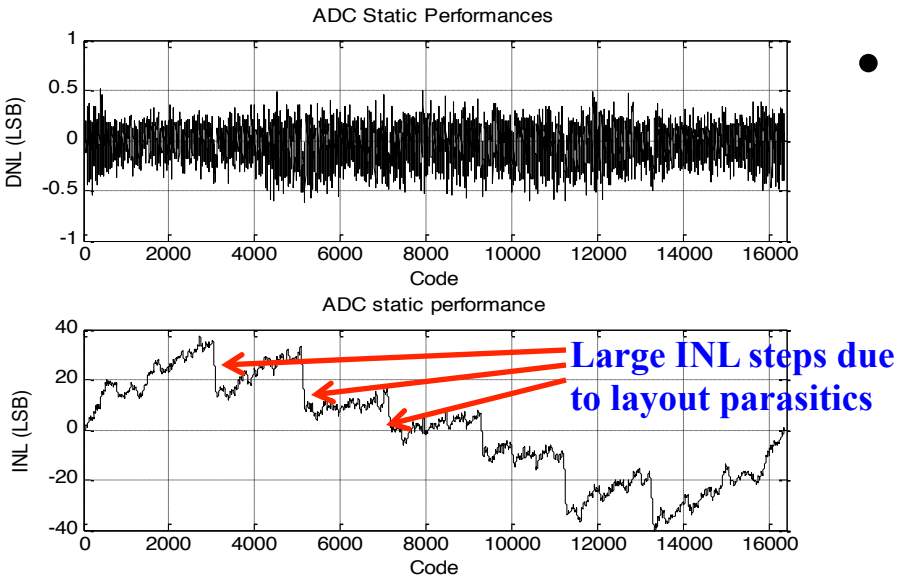
Test & Data Acquisition Board



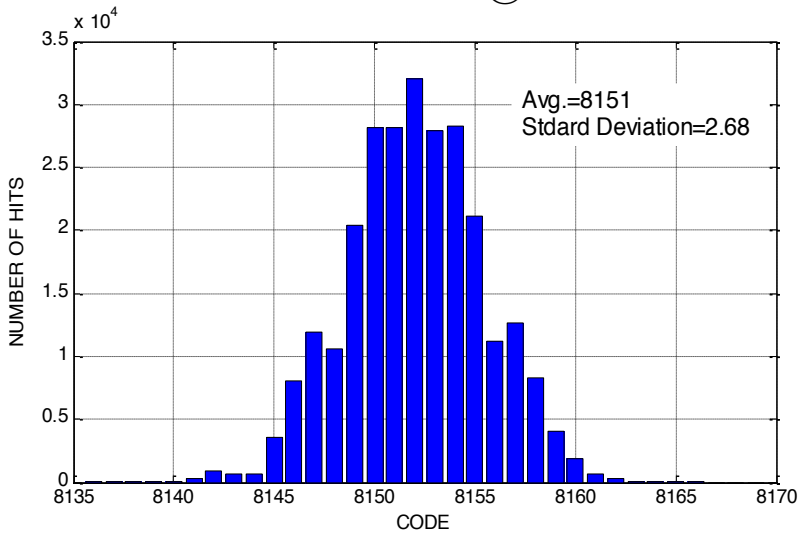


Test Board:
Eight layer board
Output bus is fully differential and has equal length
Single ground plane
Heat Dissipation

Test results of the 2nd version



Static nonlinearities @ 14-bit level

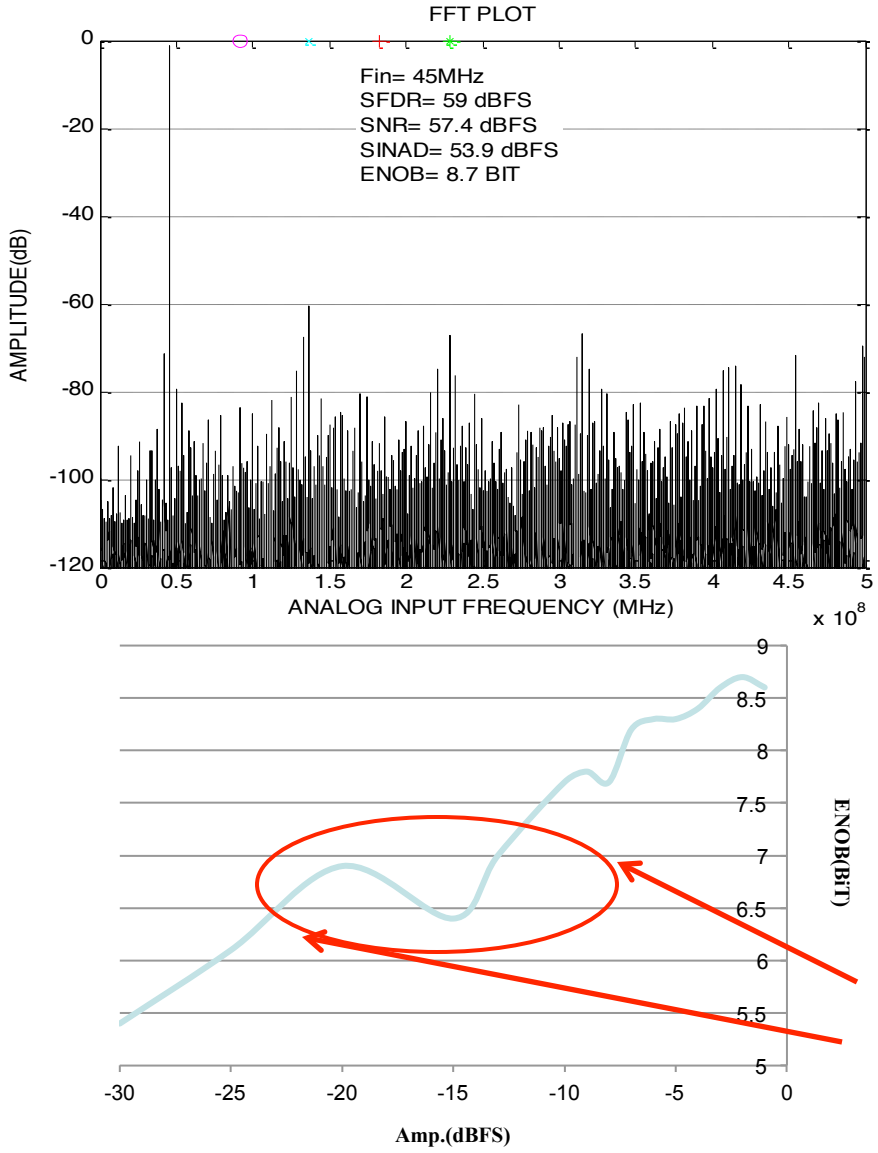


Output histogram with zero input

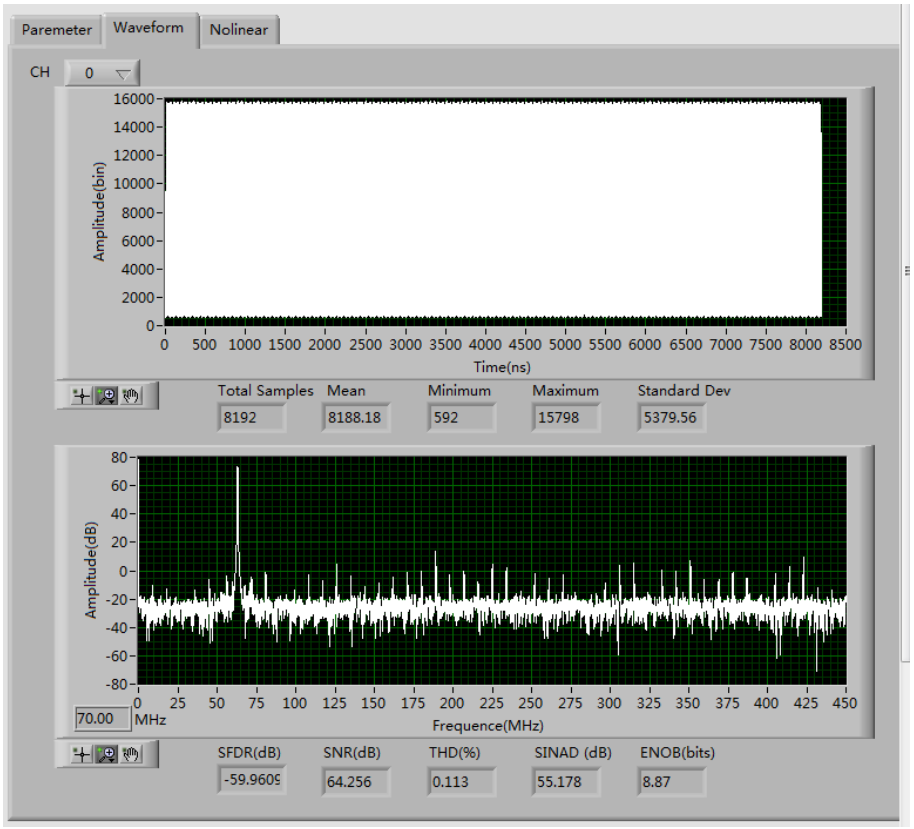
- **Static nonlinearity:**
  - The ADC accuracy is very sensitive to layout parasitics.
  - Layout parasitics extraction accuracy is limited.
  - The real measurement results may be different from post-layout simulation.
- **Zero input histogram:**
  - Standard Deviation decreased from 3.4LSB→2.7LSB. Circuit noise is optimized (vs. 1st version).

by Li Fule

Dynamic performance



- **ENOB 8.7bit@fin=45MHz**



Limited dynamic performance due to poor INL

Test Summary of the 2nd version

- **Successful: Complete 1 GS/s A/D conversion function has been achieved.**
- **The following incorrect modules in 1st edition have been corrected:**
  1. **SPI**
  2. **LVDS**
- **Unsuccessful: A/D conversion linearity is worse than that of 1st edition due to increased layout parasitics.**
- **Solution: Calibrate the effect of parasitics in digital part according to the measured inter-stage gain errors.**

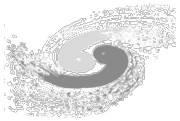
Main optimization points in the 3rd version

- **According to the test results, to optimize the circuit and layout as follows**

Num.	Description
1	Adjusting the output data sampling edge to make the output timing more reasonable
2	Adding output mode to calibrate linearity errors via SPI
3	Optimizing circuit design to break the existing speed bottleneck
4	Shielding the critical nodes to decrease the gain error due to layout parasitic
5	Strengthening internal power supply and signal routing to relieve IR drop and parasitic effect
6	Improving internal signal driving ability and decoupling
∘ ∘ ∘	∘ ∘ ∘

Tapeout on 12 Oct. 2016
200~400 chips will be available for reliability test in Dec. 2016 according to the plan (in Hu Jun's & Ning Zhe's talk)

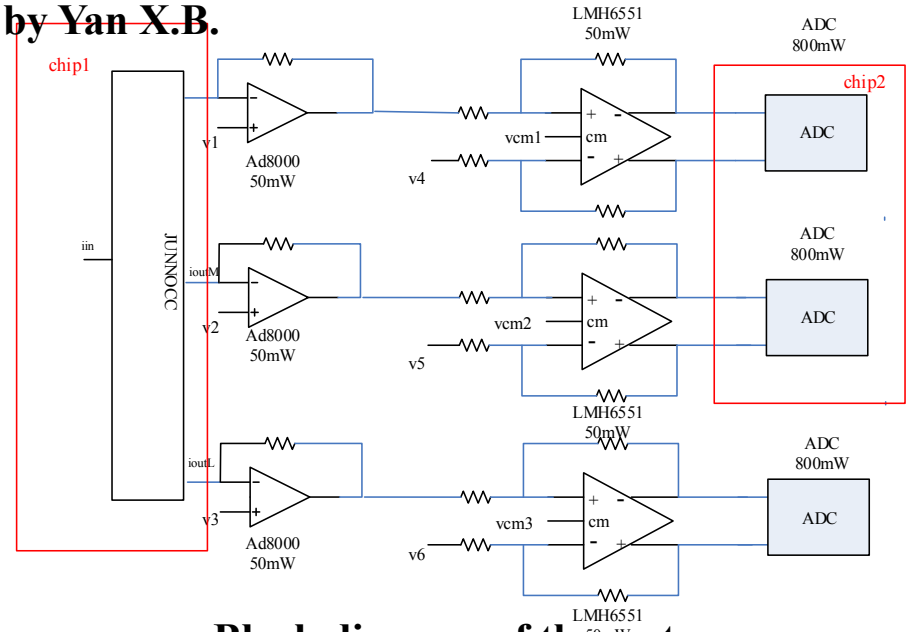
Ideas of Multiple chips in one package



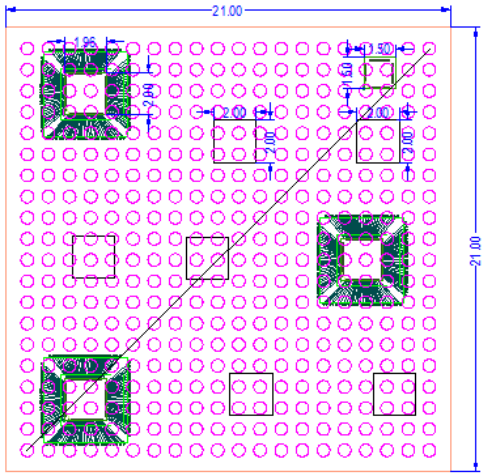
- **Problems of current design if using conventional package**
  - **2 Tsinghua ADCs per PMT**
    - **QFN68 with 8mm*8mm size**
    - **14 pairs of high speed LVDS with equal length requirement**
    - **Area consuming in PCB design, limited space in the PMT house**
  - **Conventional packages are not heat optimized**
    - **Most are plastic package, not good for heat dissip.**
    - **TIA and ADC are both power consuming devices**
  - **Multiple packages lower down the reliability**
    - **Possibilities of multiple points failure**
- **Trying to integrated FEC (by Xiongbo) & 2/3 Tsinghua ADCs in one package (System-in-Package, SIP)**
  - **Must be highly reliable package**
  - **Heat optimized**
  - **Help for high speed performance and interconnection**

Ideas of SIP

by Yan X.B.



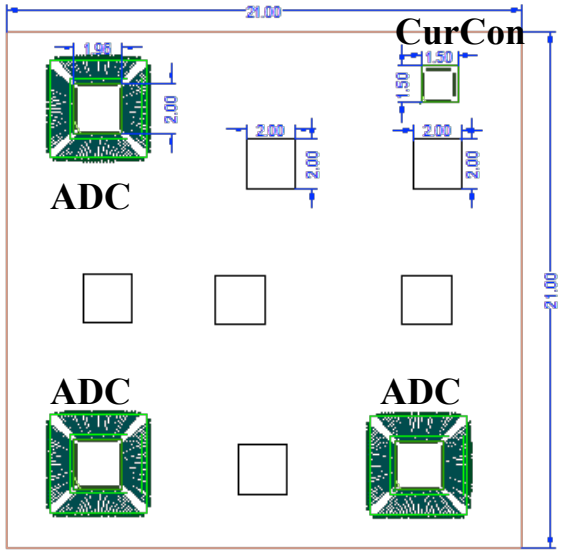
Block diagram of the system

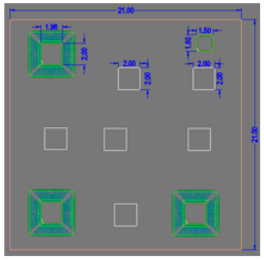


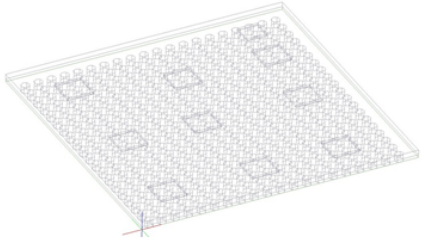
1st floorplan of the SIP

- System architecture: FEC+ADC
  - Current conveyor (100mW) + TIA (50mW) + Sing.-to-Diff. (50mW) + Tsinghua ADC (800mW)
    - 2 gain range for PMT
    - TBD: 1 spare ADC for redundancy for the small signal range
    - TIA (AD8000) and Sing.-to-Diff. amplifiers are bare dies from commercial devices
- For SIP
  - Co-design with the top level packaging company
  - All 10 dies(max.) are packed in one BGA package(21mm*21mm)
  - Interconn. on organic/ceramic substrate

Ideas of SIP

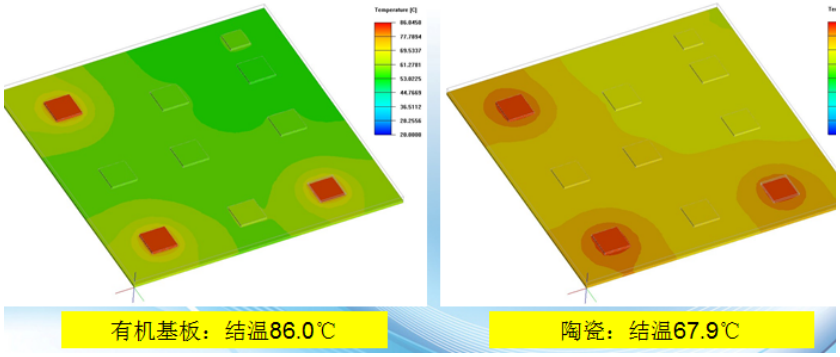






Package Design

仿真模型



有机基板：结温86.0℃

陶瓷：结温67.9℃

- **High reliability**
  - **Multiple points failure ➞ single point**
  - **All interconn. based on mature IC technology**
- **Ease the PCB design, help for performance**
  - **All interconn. as short as possible**
  - **All interconn. on substrate, less LC than in PCB**
  - **Single BGA package on PCB, less area, less fanout**
- **Heat simulatation as the 1st step**
  - **Junc. temp. 86.0℃ for organic and 67.9℃ for ceramic substrate as simulated**
  - **Further optimization on-going**
  - **Can junc. temp. be as low as 30 ℃?**

Thank you !