

GCU Firmware Trigger and Timing

M. Bellato, A. Bergnoli, R. Brugnera, D. Corti, A. Garfagnini, J. Hu,
R. Isocrate, I. Lippi, D. Pedretti

INFN and University of Padova

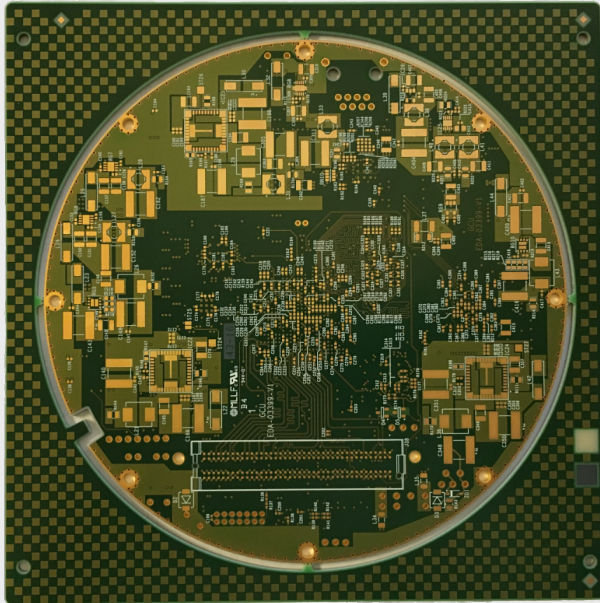
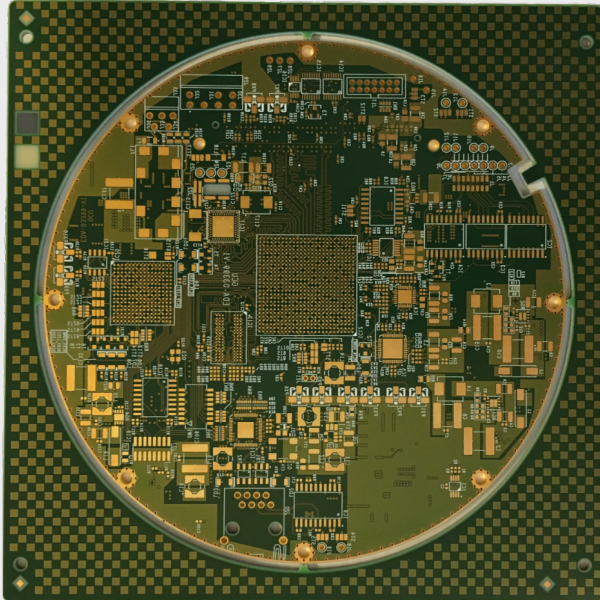


UNIVERSITÀ
DEGLI STUDI
DI PADOVA

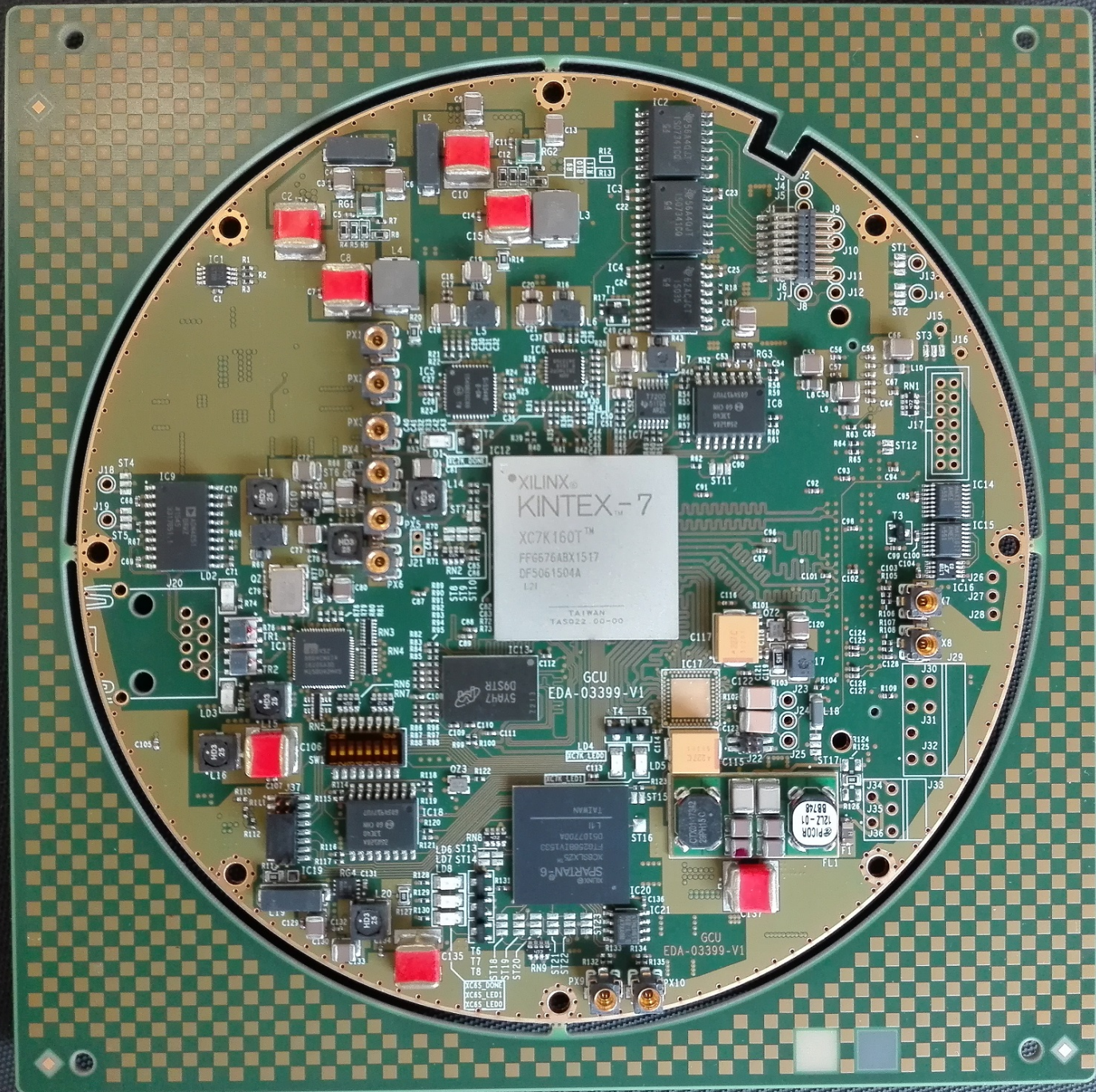
Outline

- GCU hardware status and time schedule
- Firmware Overview
- Management Software Overview
- IPBUS and Remote Debugging - Xilinx Virtual Cable
- Trigger Overview
- Timing and Clock Synchronization

Hardware Status



- PCBs arrived on 2nd of November
- Now being assembled at an external company
 - Delivery foreseen for this week
 - Waiting for a picture ...
- Power on tests will start next week
- Complete test with custom firmware immediately after

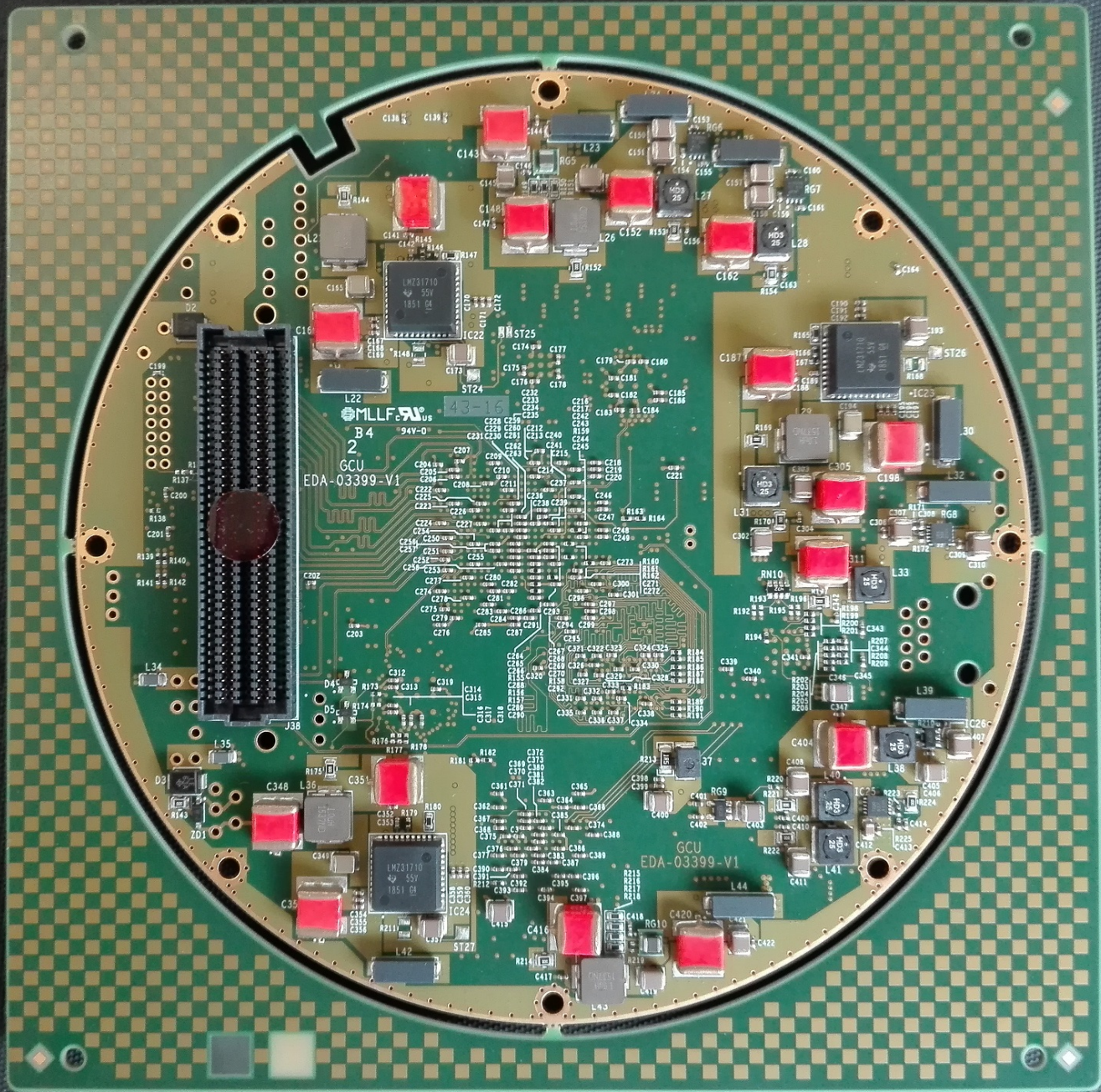


XILINX
KINTEX-7
XC7K160T™
FFG676ABX1S17
DF5061504A
L21
TAIWAN
TAS022 00-00

GCU
EDA-03399-V1

SPARTAN-6

GCU
EDA-03399-V1



C138 C139

C143

C144 C145 C146 C147

C148 C149

C150 C151 C152 C153 C154 C155 C156 C157 C158 C159

C160 C161 C162 C163 C164

C165 C166 C167 C168 C169 C170 C171 C172 C173 C174 C175 C176 C177 C178 C179 C180 C181 C182 C183 C184 C185 C186 C187 C188 C189 C190 C191 C192 C193 C194 C195 C196 C197 C198 C199 C200 C201 C202 C203 C204 C205 C206 C207 C208 C209 C210 C211 C212 C213 C214 C215 C216 C217 C218 C219 C220 C221 C222 C223 C224 C225 C226 C227 C228 C229 C230 C231 C232 C233 C234 C235 C236 C237 C238 C239 C240 C241 C242 C243 C244 C245 C246 C247 C248 C249 C250 C251 C252 C253 C254 C255 C256 C257 C258 C259 C260 C261 C262 C263 C264 C265 C266 C267 C268 C269 C270 C271 C272 C273 C274 C275 C276 C277 C278 C279 C280 C281 C282 C283 C284 C285 C286 C287 C288 C289 C290 C291 C292 C293 C294 C295 C296 C297 C298 C299 C300 C301 C302 C303 C304 C305 C306 C307 C308 C309 C310 C311 C312 C313 C314 C315 C316 C317 C318 C319 C320 C321 C322 C323 C324 C325 C326 C327 C328 C329 C330 C331 C332 C333 C334 C335 C336 C337 C338 C339 C340 C341 C342 C343 C344 C345 C346 C347 C348 C349 C350 C351 C352 C353 C354 C355 C356 C357 C358 C359 C360 C361 C362 C363 C364 C365 C366 C367 C368 C369 C370 C371 C372 C373 C374 C375 C376 C377 C378 C379 C380 C381 C382 C383 C384 C385 C386 C387 C388 C389 C390 C391 C392 C393 C394 C395 C396 C397 C398 C399 C400 C401 C402 C403 C404 C405 C406 C407 C408 C409 C410 C411 C412 C413 C414 C415 C416

L22

B4

GCU

EDA-03399-V1

94V-D

D4 D5

J38

L34

L35

L36

L37

L38

L39

L40

L41

L42

L43

L44

L45

L46

L47

L48

R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 R30 R31 R32 R33 R34 R35 R36 R37 R38 R39 R40 R41 R42 R43 R44 R45 R46 R47 R48 R49 R50 R51 R52 R53 R54 R55 R56 R57 R58 R59 R60 R61 R62 R63 R64 R65 R66 R67 R68 R69 R70 R71 R72 R73 R74 R75 R76 R77 R78 R79 R80 R81 R82 R83 R84 R85 R86 R87 R88 R89 R90 R91 R92 R93 R94 R95 R96 R97 R98 R99 R100 R101 R102 R103 R104 R105 R106 R107 R108 R109 R110 R111 R112 R113 R114 R115 R116 R117 R118 R119 R120 R121 R122 R123 R124 R125 R126 R127 R128 R129 R130 R131 R132 R133 R134 R135 R136 R137 R138 R139 R140 R141 R142 R143 R144 R145 R146 R147 R148 R149 R150 R151 R152 R153 R154 R155 R156 R157 R158 R159 R160 R161 R162 R163 R164 R165 R166 R167 R168 R169 R170 R171 R172 R173 R174 R175 R176 R177 R178 R179 R180 R181 R182 R183 R184 R185 R186 R187 R188 R189 R190 R191 R192 R193 R194 R195 R196 R197 R198 R199 R200 R201 R202 R203 R204 R205 R206 R207 R208 R209 R210 R211 R212 R213 R214 R215 R216 R217 R218 R219 R220 R221 R222 R223 R224 R225 R226 R227 R228 R229 R230 R231 R232 R233 R234 R235 R236 R237 R238 R239 R240 R241 R242 R243 R244 R245 R246 R247 R248 R249 R250 R251 R252 R253 R254 R255 R256 R257 R258 R259 R260 R261 R262 R263 R264 R265 R266 R267 R268 R269 R270 R271 R272 R273 R274 R275 R276 R277 R278 R279 R280 R281 R282 R283 R284 R285 R286 R287 R288 R289 R290 R291 R292 R293 R294 R295 R296 R297 R298 R299 R300 R301 R302 R303 R304 R305 R306 R307 R308 R309 R310 R311 R312 R313 R314 R315 R316 R317 R318 R319 R320 R321 R322 R323 R324 R325 R326 R327 R328 R329 R330 R331 R332 R333 R334 R335 R336 R337 R338 R339 R340 R341 R342 R343 R344 R345 R346 R347 R348 R349 R350 R351 R352 R353 R354 R355 R356 R357 R358 R359 R360 R361 R362 R363 R364 R365 R366 R367 R368 R369 R370 R371 R372 R373 R374 R375 R376 R377 R378 R379 R380 R381 R382 R383 R384 R385 R386 R387 R388 R389 R390 R391 R392 R393 R394 R395 R396 R397 R398 R399 R400 R401 R402 R403 R404 R405 R406 R407 R408 R409 R410 R411 R412 R413 R414 R415 R416 R417 R418 R419 R420 R421 R422 R423 R424 R425 R426 R427 R428 R429 R430 R431 R432 R433 R434 R435 R436 R437 R438 R439 R440 R441 R442 R443 R444 R445 R446 R447 R448 R449 R450 R451 R452 R453 R454 R455 R456 R457 R458 R459 R460 R461 R462 R463 R464 R465 R466 R467 R468 R469 R470 R471 R472 R473 R474 R475 R476 R477 R478 R479 R480 R481 R482 R483 R484 R485 R486 R487 R488 R489 R490 R491 R492 R493 R494 R495 R496 R497 R498 R499 R500 R501 R502 R503 R504 R505 R506 R507 R508 R509 R510 R511 R512 R513 R514 R515 R516 R517 R518 R519 R520 R521 R522 R523 R524 R525 R526 R527 R528 R529 R530 R531 R532 R533 R534 R535 R536 R537 R538 R539 R540 R541 R542 R543 R544 R545 R546 R547 R548 R549 R550 R551 R552 R553 R554 R555 R556 R557 R558 R559 R560 R561 R562 R563 R564 R565 R566 R567 R568 R569 R570 R571 R572 R573 R574 R575 R576 R577 R578 R579 R580 R581 R582 R583 R584 R585 R586 R587 R588 R589 R590 R591 R592 R593 R594 R595 R596 R597 R598 R599 R600 R601 R602 R603 R604 R605 R606 R607 R608 R609 R610 R611 R612 R613 R614 R615 R616 R617 R618 R619 R620 R621 R622 R623 R624 R625 R626 R627 R628 R629 R630 R631 R632 R633 R634 R635 R636 R637 R638 R639 R640 R641 R642 R643 R644 R645 R646 R647 R648 R649 R650 R651 R652 R653 R654 R655 R656 R657 R658 R659 R660 R661 R662 R663 R664 R665 R666 R667 R668 R669 R670 R671 R672 R673 R674 R675 R676 R677 R678 R679 R680 R681 R682 R683 R684 R685 R686 R687 R688 R689 R690 R691 R692 R693 R694 R695 R696 R697 R698 R699 R700 R701 R702 R703 R704 R705 R706 R707 R708 R709 R710 R711 R712 R713 R714 R715 R716 R717 R718 R719 R720 R721 R722 R723 R724 R725 R726 R727 R728 R729 R730 R731 R732 R733 R734 R735 R736 R737 R738 R739 R740 R741 R742 R743 R744 R745 R746 R747 R748 R749 R750 R751 R752 R753 R754 R755 R756 R757 R758 R759 R760 R761 R762 R763 R764 R765 R766 R767 R768 R769 R770 R771 R772 R773 R774 R775 R776 R777 R778 R779 R780 R781 R782 R783 R784 R785 R786 R787 R788 R789 R790 R791 R792 R793 R794 R795 R796 R797 R798 R799 R800 R801 R802 R803 R804 R805 R806 R807 R808 R809 R810 R811 R812 R813 R814 R815 R816 R817 R818 R819 R820 R821 R822 R823 R824 R825 R826 R827 R828 R829 R830 R831 R832 R833 R834 R835 R836 R837 R838 R839 R840 R841 R842 R843 R844 R845 R846 R847 R848 R849 R850 R851 R852 R853 R854 R855 R856 R857 R858 R859 R860 R861 R862 R863 R864 R865 R866 R867 R868 R869 R870 R871 R872 R873 R874 R875 R876 R877 R878 R879 R880 R881 R882 R883 R884 R885 R886 R887 R888 R889 R890 R891 R892 R893 R894 R895 R896 R897 R898 R899 R900 R901 R902 R903 R904 R905 R906 R907 R908 R909 R910 R911 R912 R913 R914 R915 R916 R917 R918 R919 R920 R921 R922 R923 R924 R925 R926 R927 R928 R929 R930 R931 R932 R933 R934 R935 R936 R937 R938 R939 R940 R941 R942 R943 R944 R945 R946 R947 R948 R949 R950 R951 R952 R953 R954 R955 R956 R957 R958 R959 R960 R961 R962 R963 R964 R965 R966 R967 R968 R969 R970 R971 R972 R973 R974 R975 R976 R977 R978 R979 R980 R981 R982 R983 R984 R985 R986 R987 R988 R989 R990 R991 R992 R993 R994 R995 R996 R997 R998 R999 R1000

L23

L26

L27

L28

L29

L30

L31

L32

L33

L34

L35

L36

L37

L38

L39

L40

L41

L42

L43

L44

L45

L46

L47

L48

L49

L50

L51

L52

L53

L54

IC22

IC23

IC24

IC25

IC26

IC27

IC28

IC29

IC30

IC31

IC32

IC33

IC34

IC35

IC36

IC37

IC38

IC39

IC40

IC41

IC42

IC43

IC44

IC45

IC46

IC47

IC48

IC49

IC50

IC51

ST24

ST25

ST26

ST27

ST28

ST29

ST30

ST31

ST32

ST33

ST34

ST35

ST36

ST37

ST38

ST39

ST40

ST41

ST42

ST43

ST44

ST45

ST46

ST47

ST48

ST49

ST50

ST51

ST52

ST53

RG5

RG6

RG7

RG8

RG9

RG10

RG11

RG12

RG13

RG14

RG15

RG16

RG17

RG18

RG19

RG20

RG21

RG22

RG23

RG24

RG25

RG26

RG27

RG28

RG29

RG30

RG31

RG32

RG33

RG34

MD5

MD6

MD7

MD8

MD9

MD10

MD11

MD12

MD13

MD14

MD15

MD16

MD17

MD18

MD19

MD20

MD21

MD22

MD23

MD24

MD25

MD26

MD27

MD28

MD29

MD30

MD31

MD32

MD33

MD34

ST25

ST26

ST27

ST28

ST29

ST30

ST31

ST32

ST33

ST34

ST35

ST36

ST37

ST38

ST39

ST40

ST41

ST42

ST43

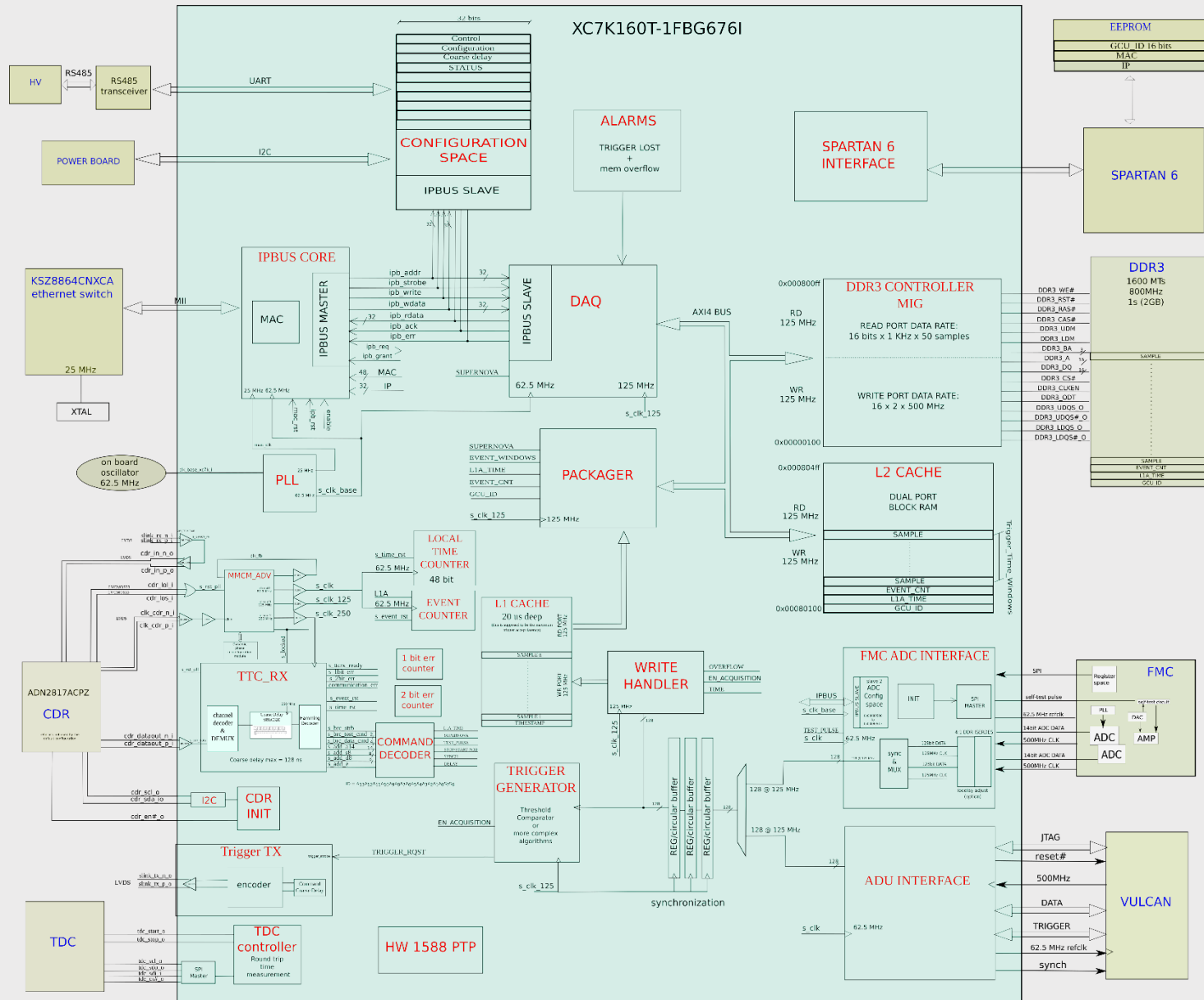
ST44

ST45

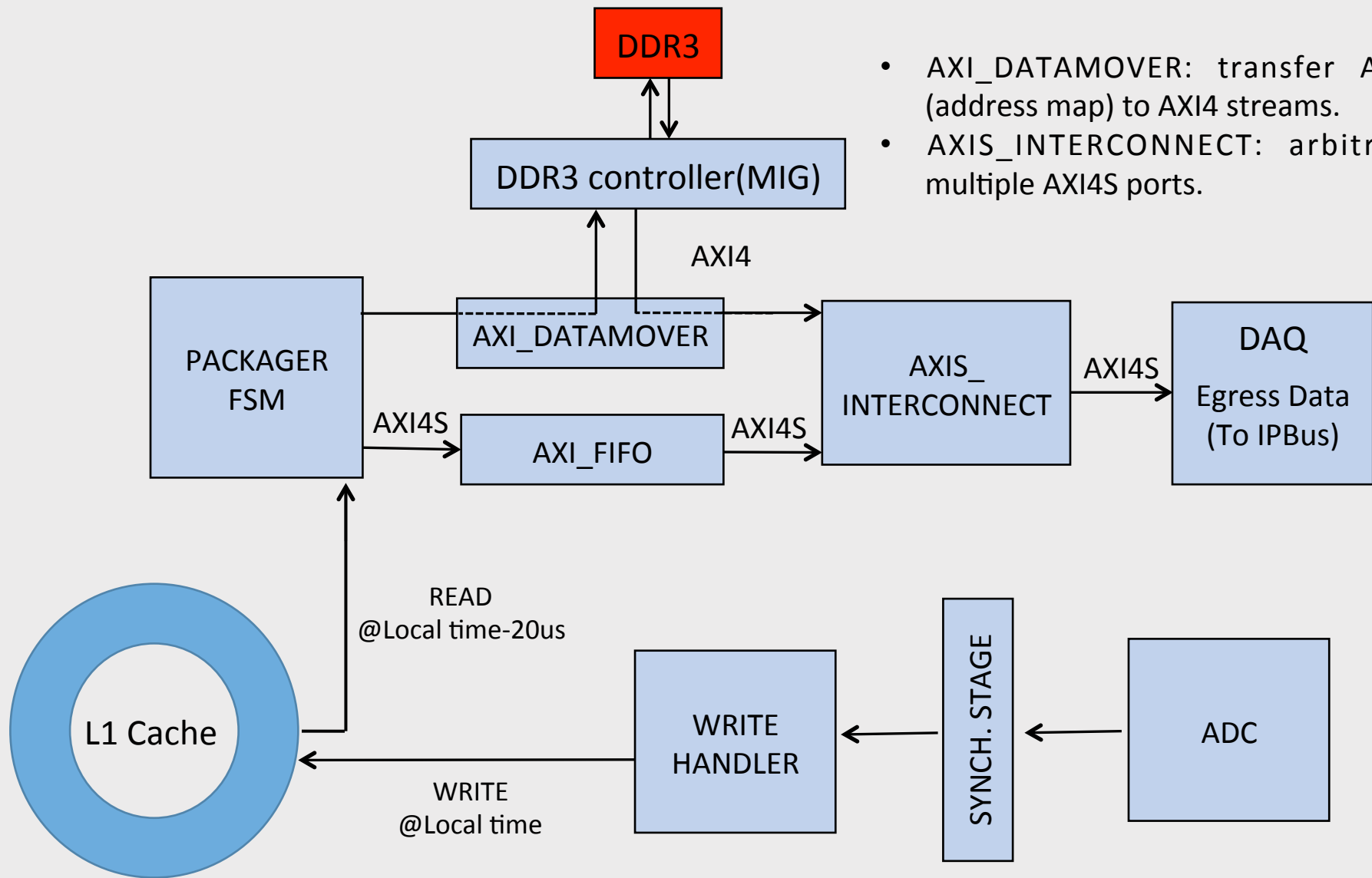
ST46

ST47

Firmware Block Diagram



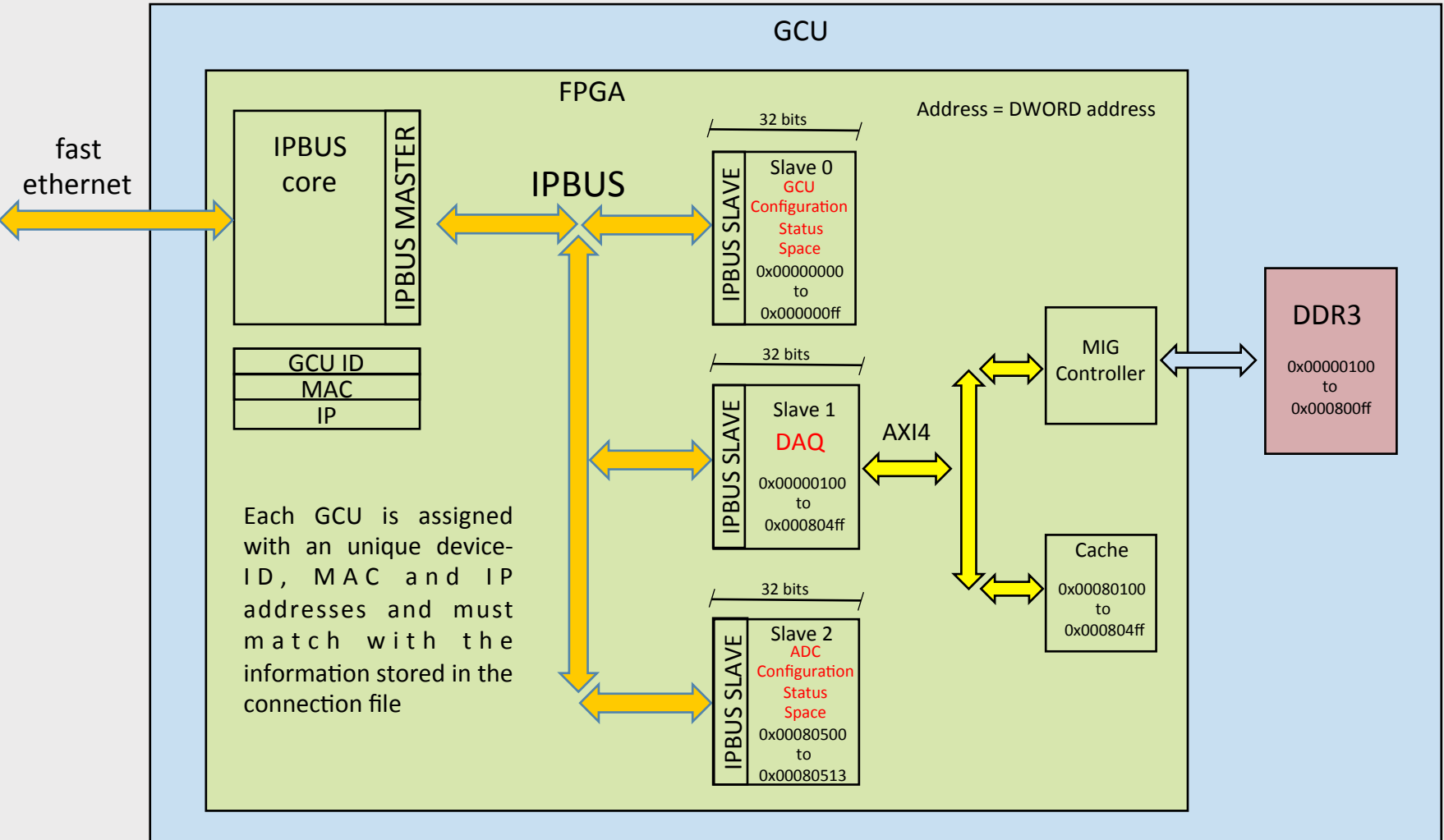
ADCs I/F and Data Readout



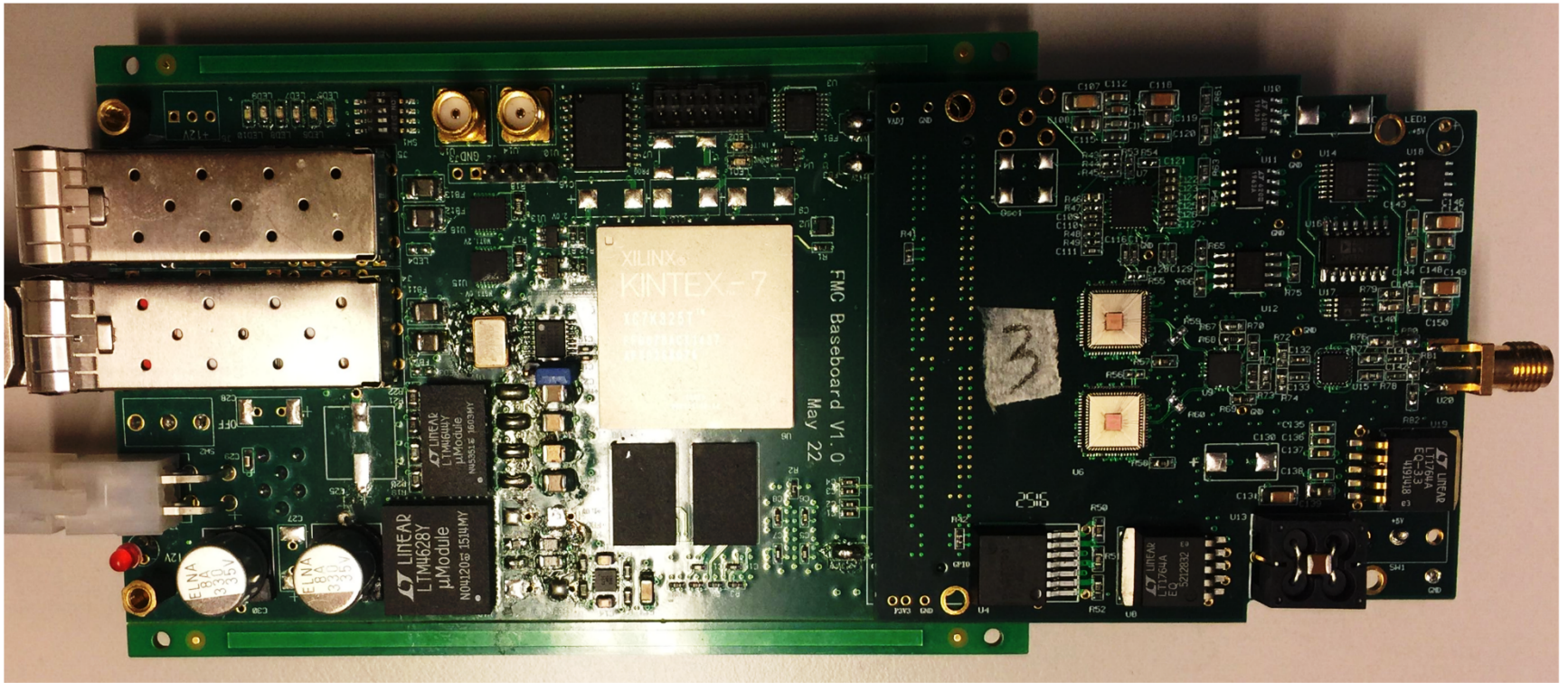
- AXI_DATAMOVER: transfer AXI4 (address map) to AXI4 streams.
- AXIS_INTERCONNECT: arbitrate multiple AXI4S ports.

Data Readout

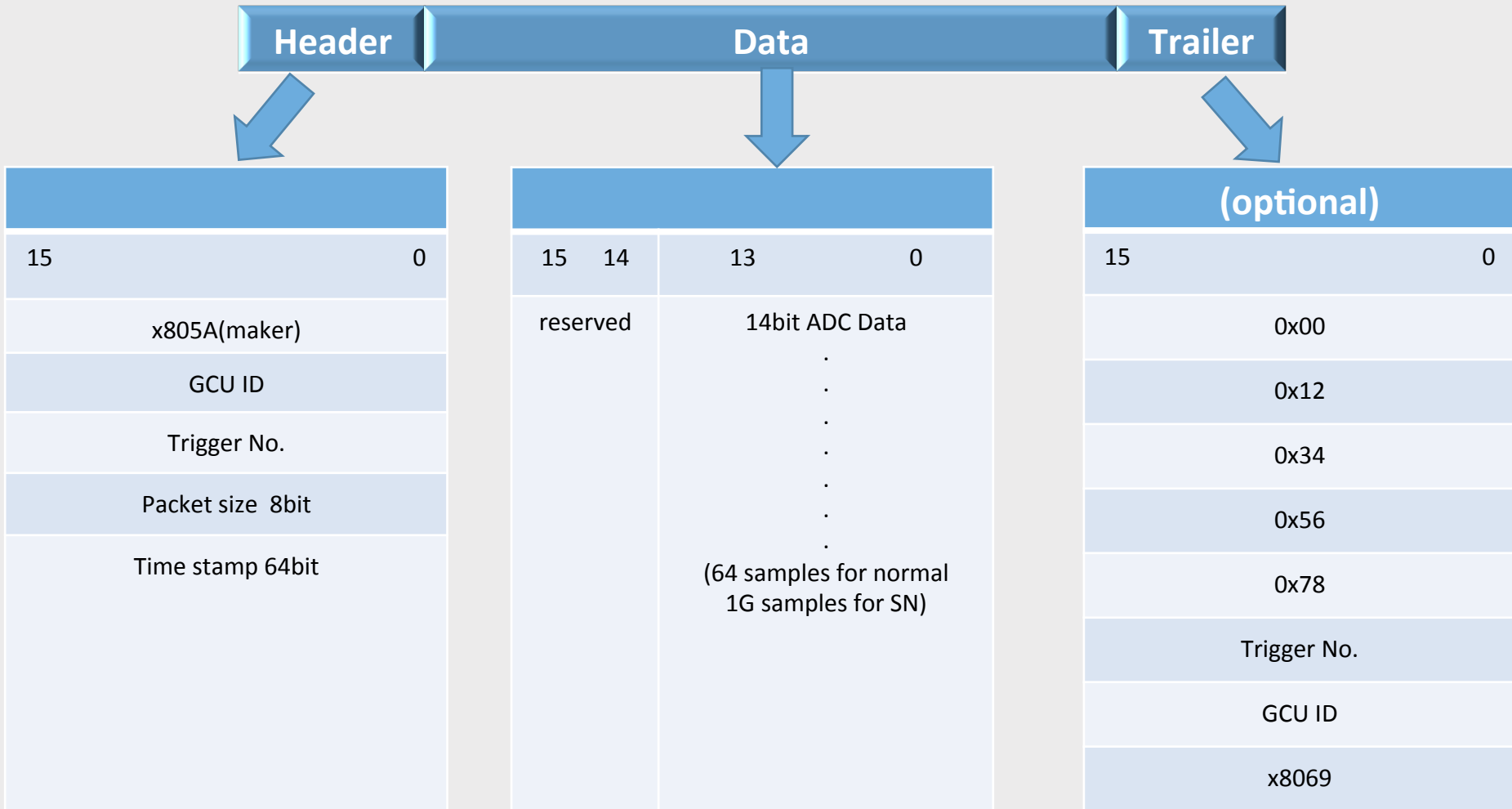
Data Readout is performed via IPBUS. The data rate achieved is ~90 Mbit/sec with block data transfers (the IPBUS efficiency increases with the payload). Accepted events are stored in the cache waiting to be pulled out by software in bunch of 5 in 5.



TsingHua ADC Test SetUp



Data Package Structure



Data Buffer Capability

- L1 Cache => Ring buffer
 - Maximum trigger latency: **20us**
 - Cache1 size = 16Gbps x 20us = **320kbits**
- L2 Cache => internal ram & DDR3
 - For internal ram (normal event)
 - Readout window width: **90 ns**
 - Event size : 128 bit header + 16bit x 90 samples ~ **1600 bits**
 - Event cache capability **20 events = 32Kbit**
 - For DDR3 (Supernova)
 - Readout window width: **1s**
 - Event size : 128 header + 16 x 1G = **2GB**
 - Event cache capability **1events = 2GB**

All the calculation is without data compression.

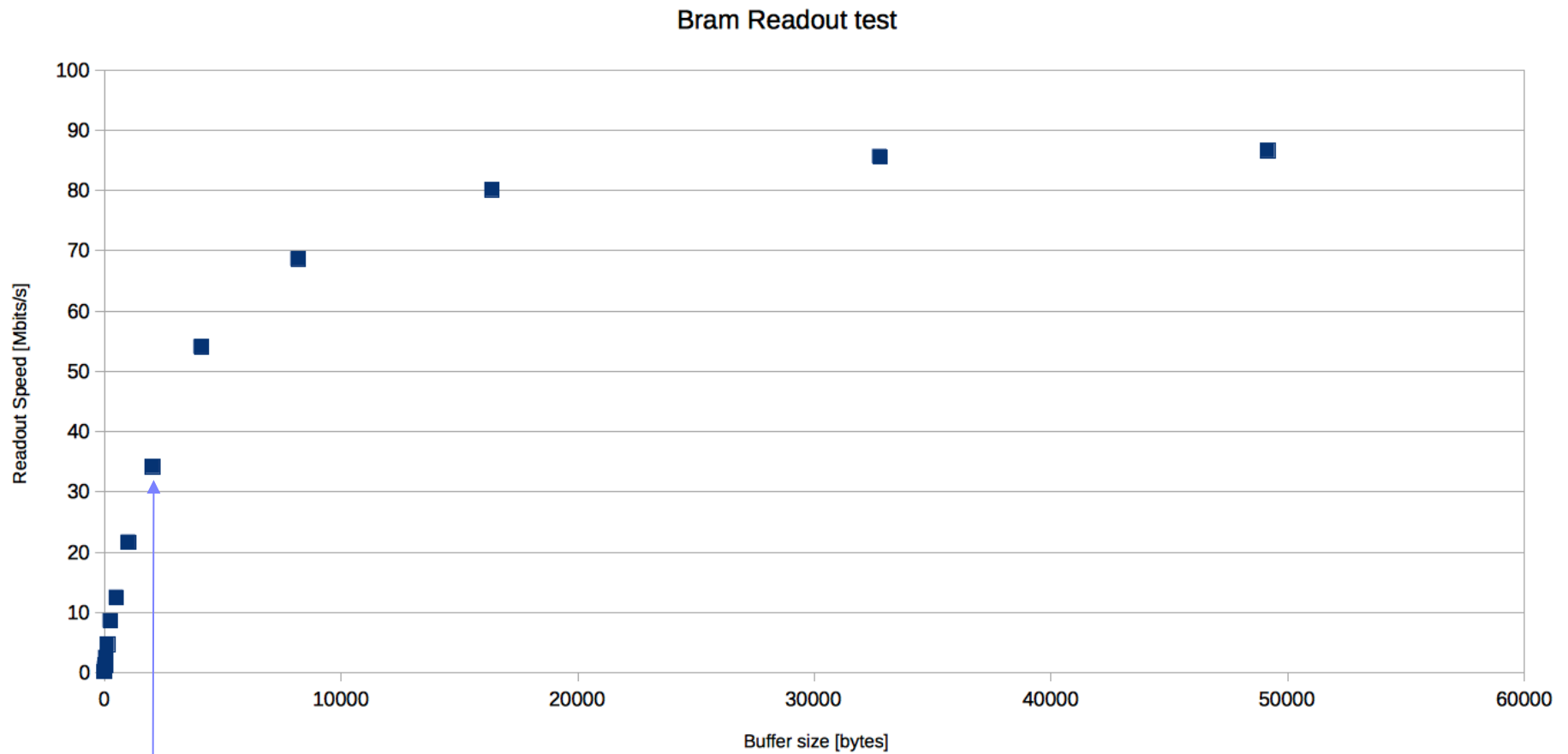
Data rate

- The raw data rate generated by ADC is **16 Gbps/1ch**
 - FMC to FPGA bandwidth is 32 Gbps(2 TsingHua ADC).
 - After selecting one out of two chips: 16 Gbps
- DDR3 write bandwidth is **800 MHz** x 16bits x 2 x 85%(efficiency) = **21.76 Gbps**
- Max Ethernet's bandwidth (IPBus) is ~ **90 Mbps**
 - Normal mode (event validation), 1600b x 1KHz = **1.6 Mb/s**
 - In Autotrigger mode : 40 samples x 16 bit x 50 KHz = **32Mb/s**

DAQ Readout tests(1)

- *IPBUS Readout works in pull mode*, e.g. Server retrieves data from GCUs memory
- *Test code reads many times from blockram instantiated in Kintex7 as IPBUS slave*
- A C++ routine reads back 10000 times a variable size buffer and measure elapsed time
- Link speed forced to 100BaseTx
- Topology: 1 ipbus client (PC) → 1 target (KC705) (no control hub)

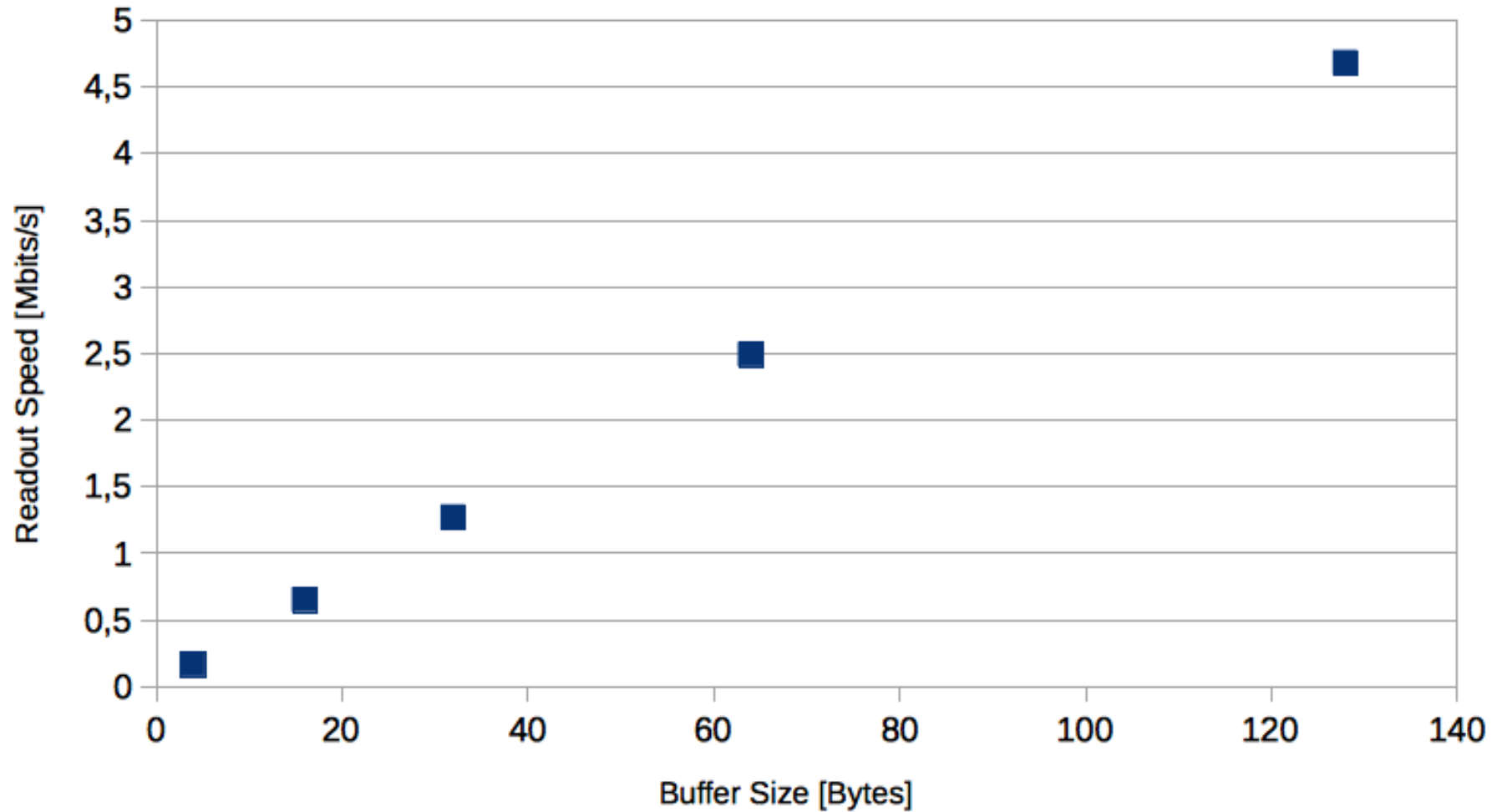
DAQ Readout tests(2)



Buffer Size = 16Kbit

DAQ Readout tests(3)

Details for smallests buffer sizes



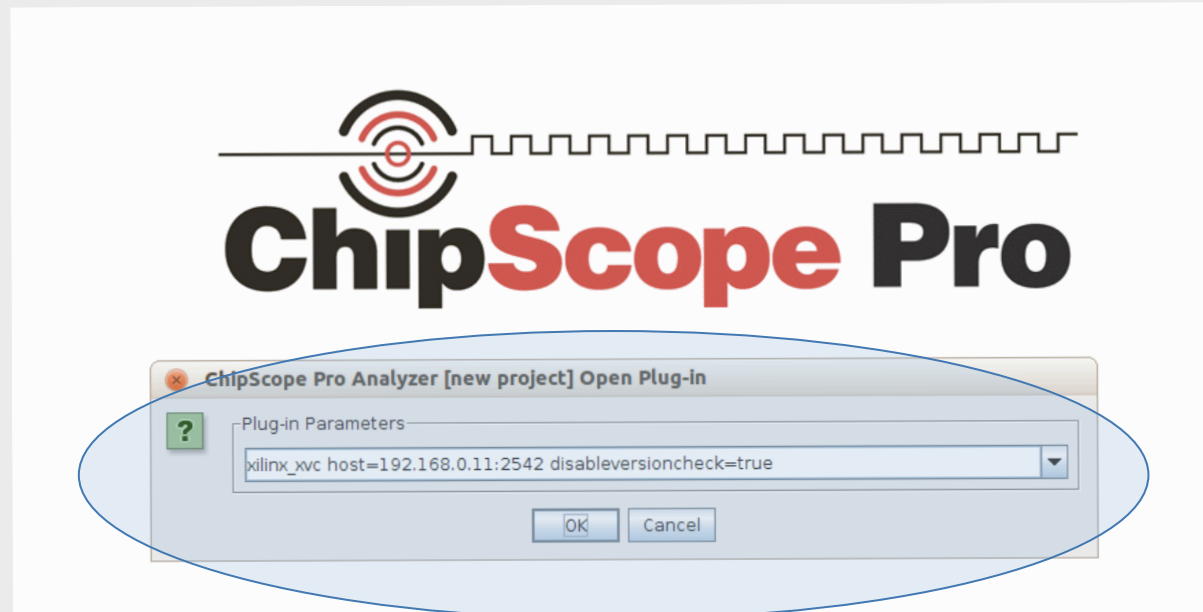
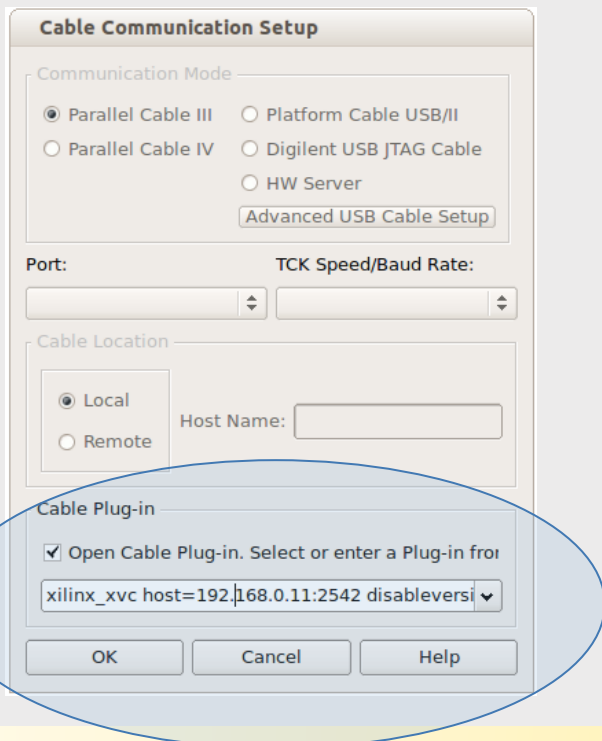
Remote debugging – Virtual JTAG over IPBUS(1)

Virtual JTAG components

- Xilinx Debug & Programming tools (***Impact***[™] and ***Chipscope***[™], also ***Vivado***[™]) are able to connect to a TCP port service named **xilinx_xvc**
- A Tcp server implementing this *xvc protocol* and able to perform ipbus operations (uhal library).
- IPBUS slave on Spartan6 (named JTAG TAP) drives TDI-TMS-TCK-[TDO] of the kintex7)

Remote debugging – Virtual JTAG over IPBUS(2)

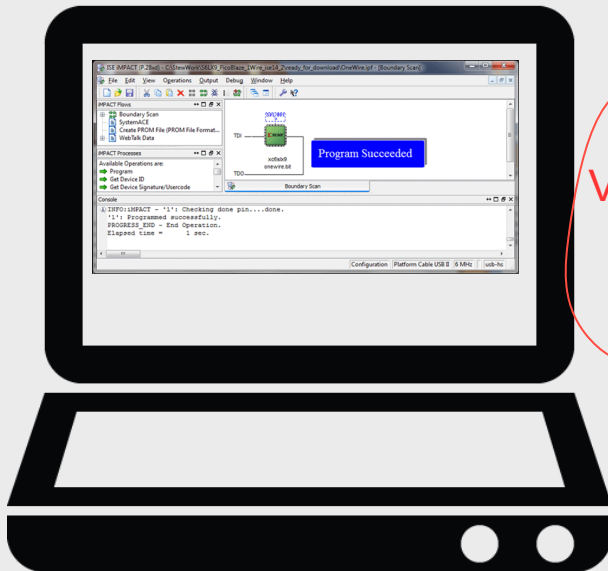
- Trivial configuration from the tools side: just specify the protocol and the address:



Remote debugging – Virtual JTAG over IPBUS(3)

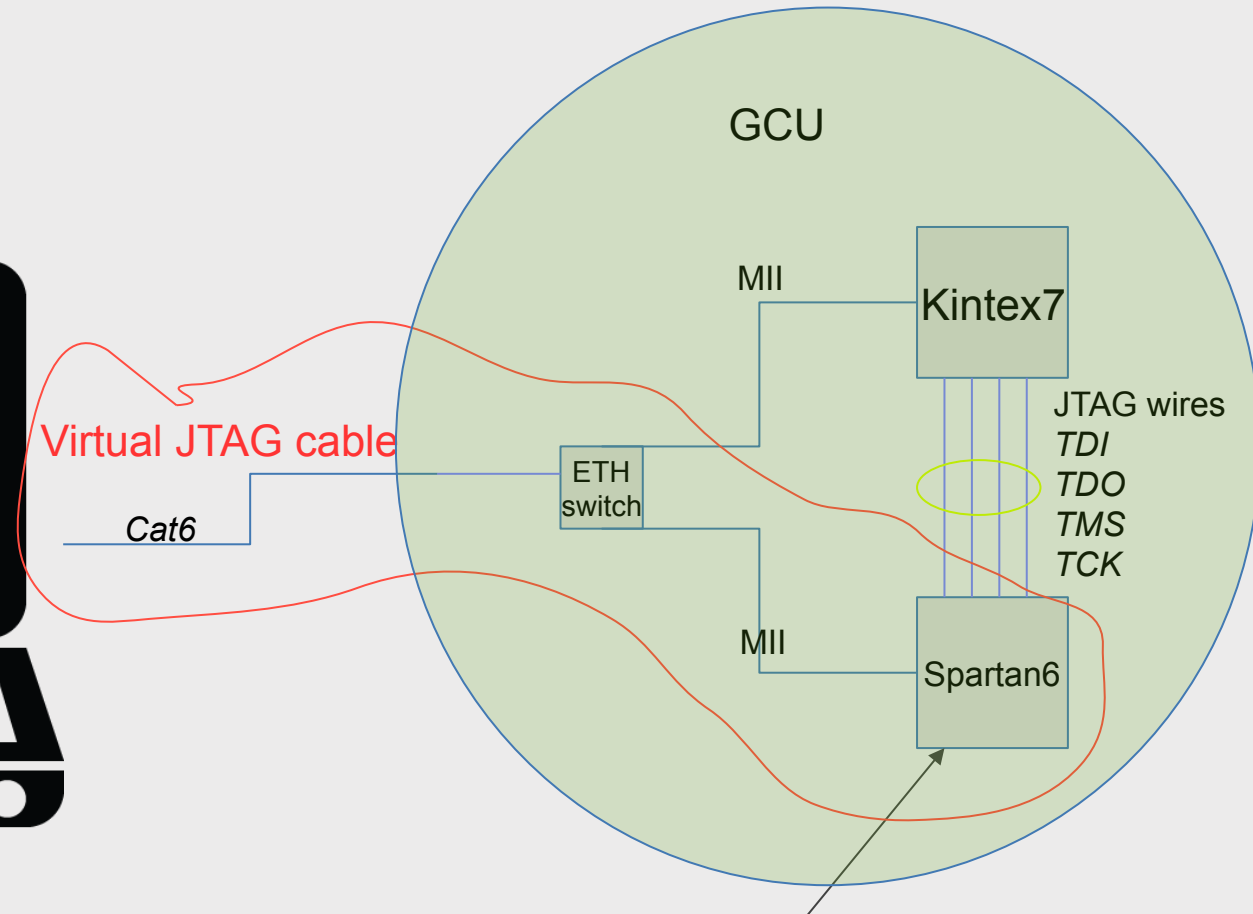
Component on PC:

- Xilinx tools
- xvc server
- uhal library → ipbus



Virtual JTAG cable

Cat6

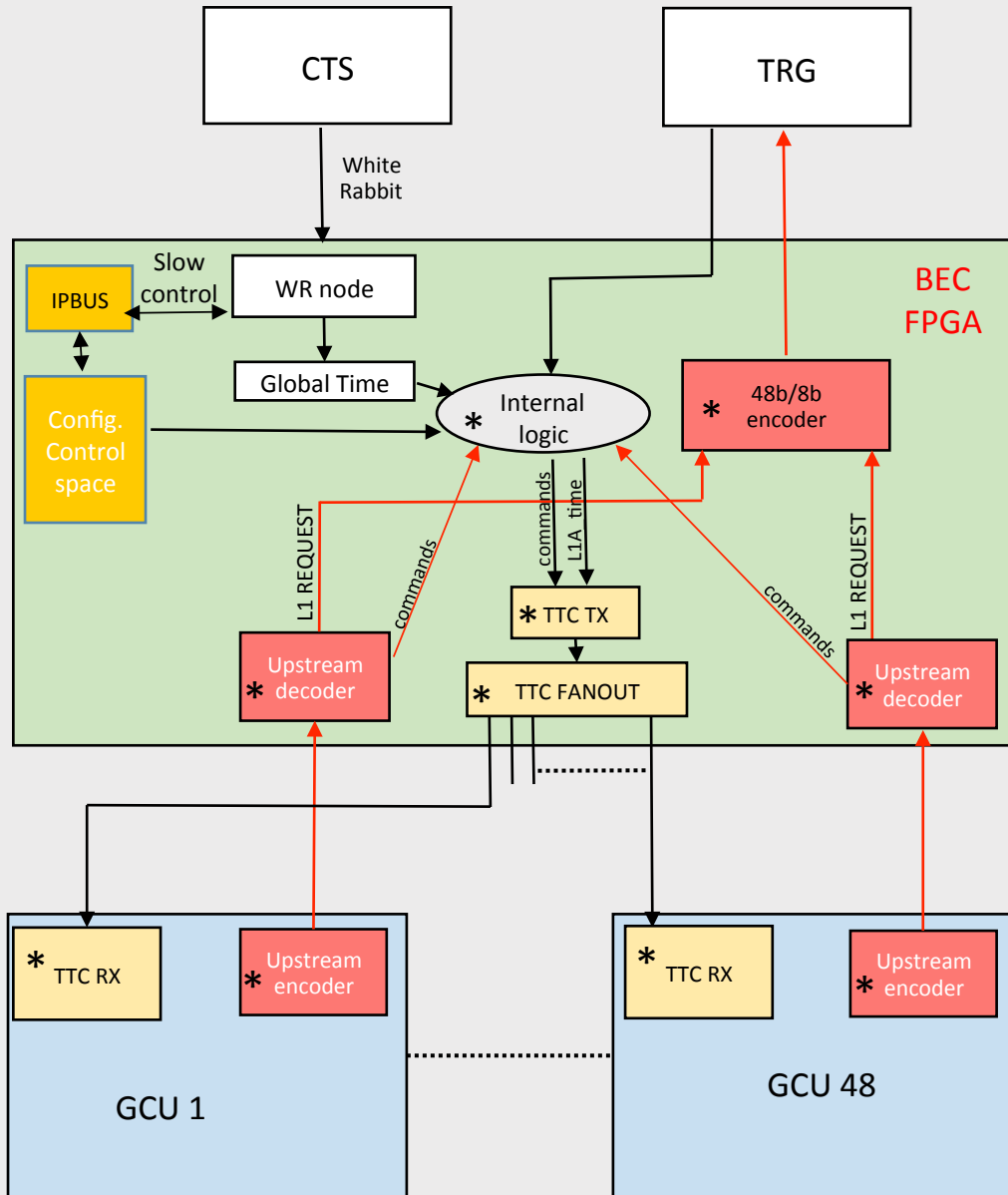


Small Spartan6 FPGA acts as *Xilinx remote cable*, IPBus slave (JTAG TAP) lives here

Current status:

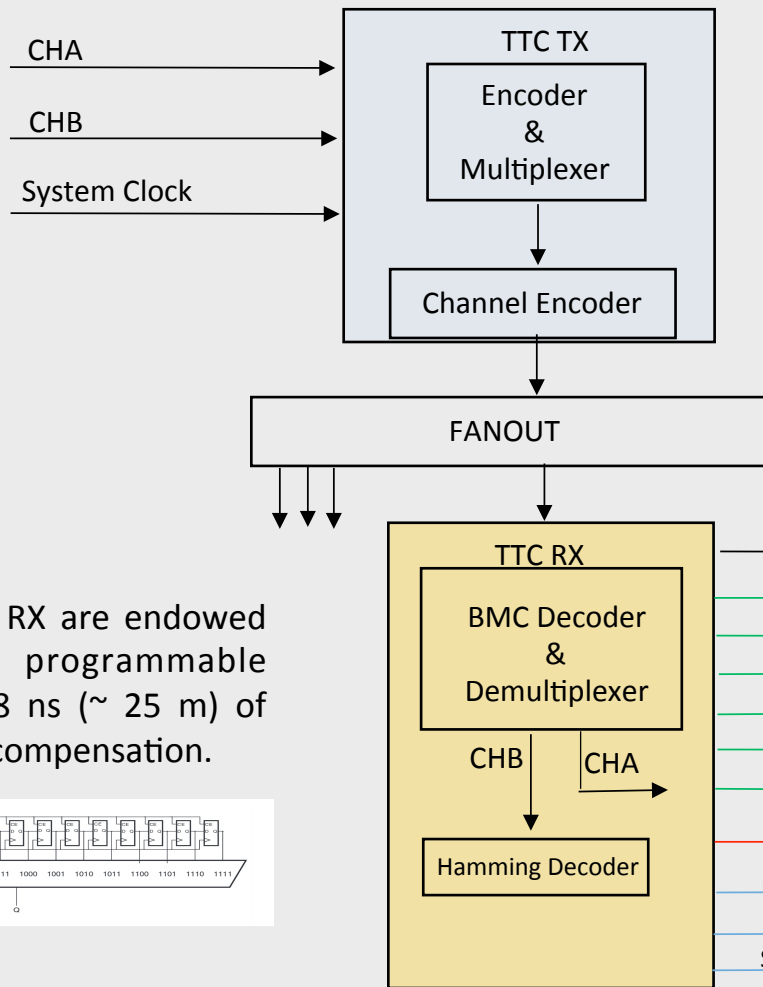
- Kc705 board successfully programmed with Impact (running on PC) + Xvc server (running in a small single board PC) able to mimic JTAG with onchip GPIO [*takes several minutes*];
- Ongoing development on IPBUS JTAG slave; simple bitbanged GPIO is very slow → The buffering defined in the XVC protocol should be exploited.

GCU Trigger Interface Overview



- Synchronous upstream trigger request channel.
- Downstream trigger validation command: asynchronous (max latency); the trigger validation command is tagged with the time windows.
- Synch links bandwidth requirement: 250 Mbps.
- The sync links downstream and upstream should not carry information only on trigger but we need to encode asynchronous and synchronous commands.
- To open the possibility to send to all the GCU synchronous command all the blocks marked with * must have a fixed latency.
- The Downstream protocol is based on CERN TTCrx/tx.
- Upstream we have to accommodate 48 decoders in the BEC FPGA; simple protocol. BEC FPGA resources issue.
- Level trigger. Trigger request information is updated every 16 ns.
- Both TTC RX as well as the upstream encoder incorporate programmable coarse delay to compensate for the electronics and cable propagation delays.

TTCrx/tx Overview

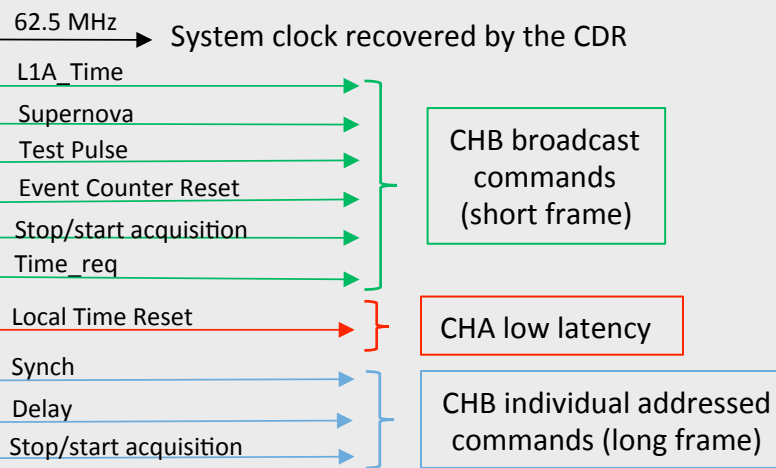
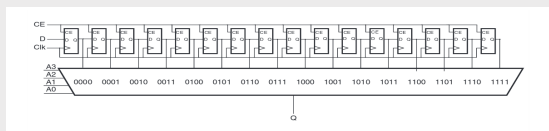


Two communication channels are Time Division Multiplexed and channel B is encoded using the Hamming code scheme.

Data stream is BiPhase Mark Encoded (BMC) before to be transmitted over the physical channel.

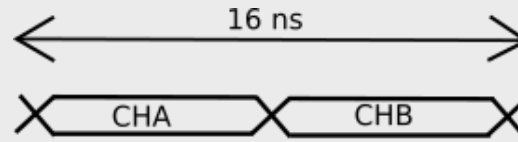
More info about the data framing at: <http://ttc.web.cern.ch/TTC/>

TTC TX and TTC RX are endowed with a coarse programmable delay; up to 128 ns (~ 25 m) of cable mismatch compensation.

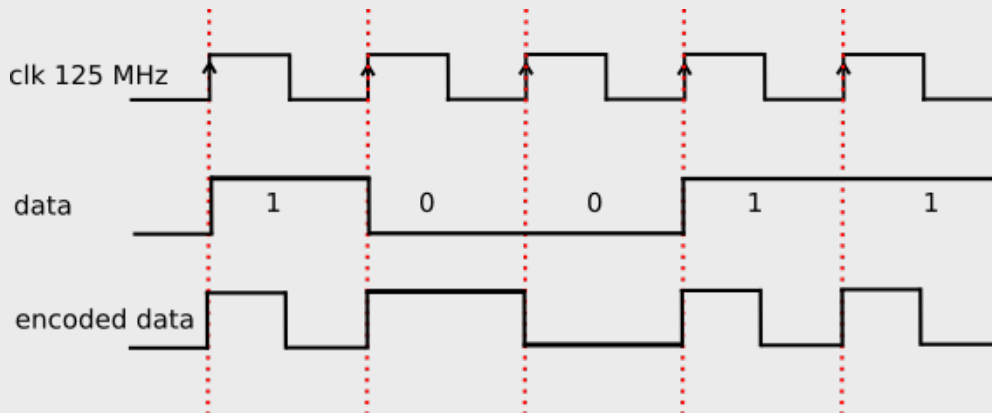


TTC – TDM and BMC

Time Division Multiplexed:



Bi-phase Mark Code:



- Transition on every rising clock edge,
- Data = 1 → bi-phase,
- Data = 0 → constant level during Tck

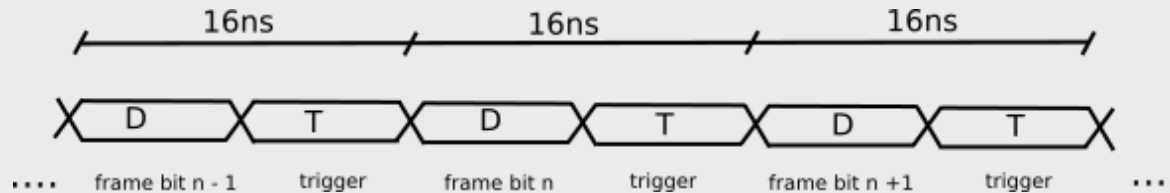
Pro and cons:
+ DC balanced
+ self-clocking
- Half channel bandwidth available

All this does not come for free! We cannot fit many TTC RX in a single FPGA therefore for the upstream channel we need a simpler protocol.

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	162	202800	0%
Number of Slice LUTs	258	101400	0%
Number of fully used LUT-FF pairs	116	304	38%
Number of bonded IOBs	53	400	13%
Number of BUFG/BUFGCTRLs	2	32	6%

Upstream Trigger Protocol

- The upstream trigger request link, from the GCU to the TRG, must be synchronous (fixed latency).
- Trigger on the level.
- Trigger request is updated every 16 ns.
- Not only trigger; we need to send to the BEC synchronous commands. Likewise TTC, the trigger request (T) is Time Division Multiplexed with the data/command frame bits (D):



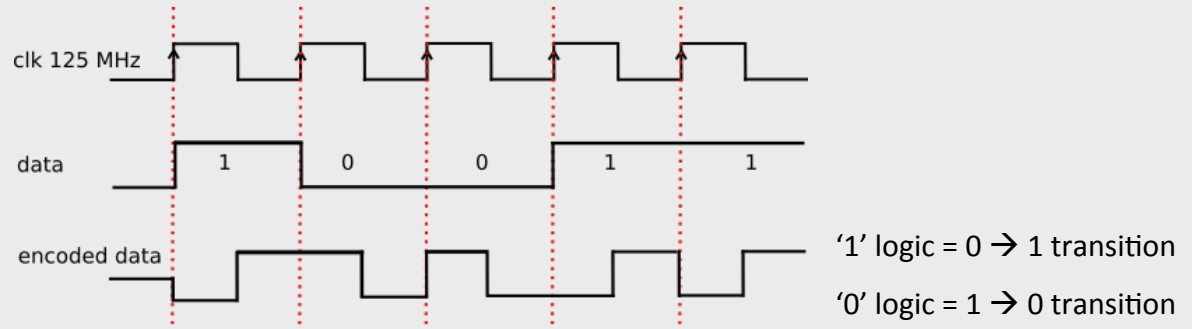
- Data framing: 1 start bit + 8 bit of data + 1 parity bit (optional) + 1 stop bit.

bit number	1	2	3	4	5	6	7	8	9	10	11
	Start	H	H	H	H	D	D	D	D	P	Stop

- Command table:

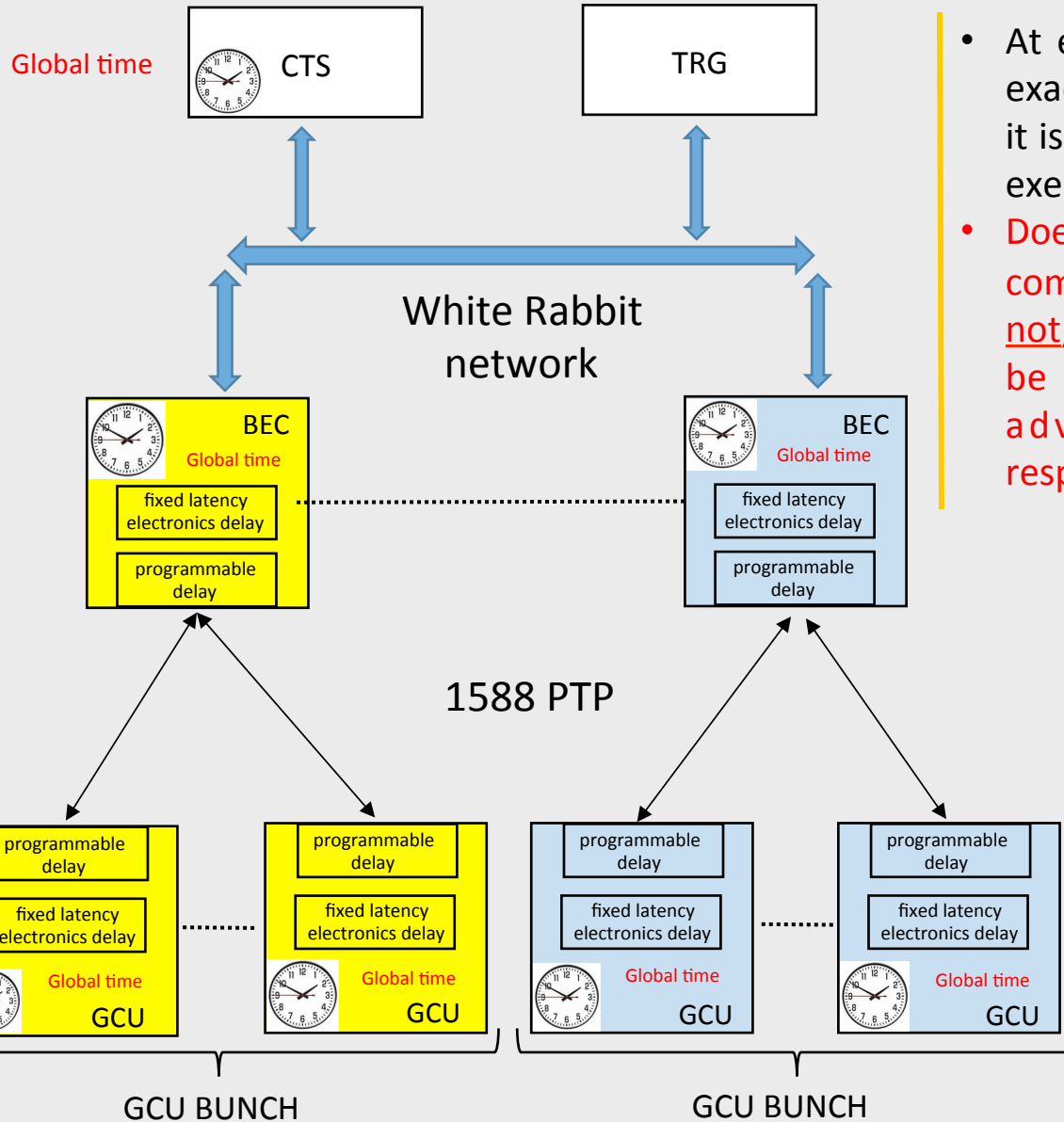
HHHH	DDDD	command
0000	0000	COMMA
0001	XXXX	BACK_PRS_ON
0010	XXXX	BACK_PRS_OFF
0011	XXXX	DELAY REQ
0100	DDDD	TIME
0101	0101	IDLE
0110	XXXX	TDB
....	TDB

- Channel encoding: Manchester (PE); it guarantees no DC bias and is self-clocking. The channel can be AC coupled.



- A doubled channel bandwidth is required.

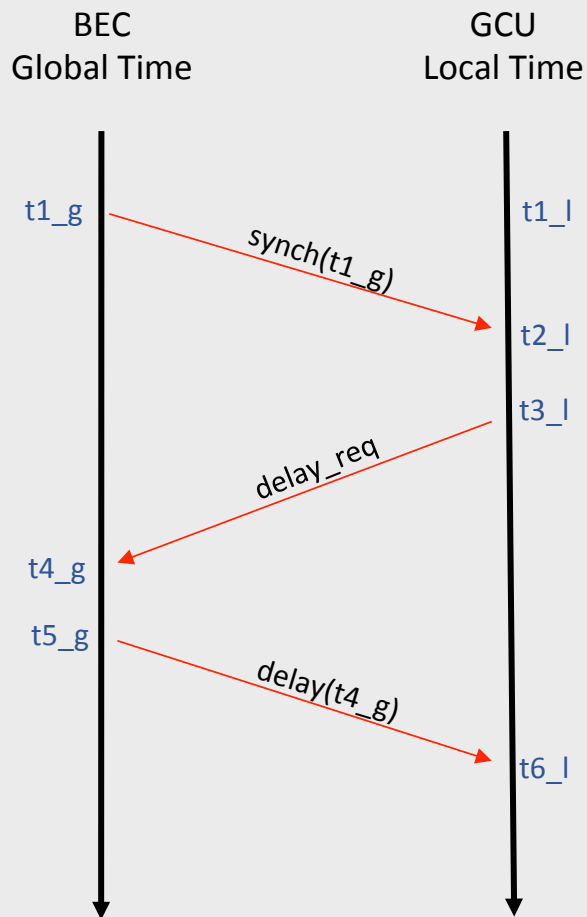
Synchronous operations



- At each level of the system there is an exact copy of the global time therefore it is possible to program all the nodes to execute synchronous operations.
- Does WR allow sending synchronous commands from TRG to all the BECs ? IF not, the synchronous operations must be predictable and programmed in advance; the system won't be responsive to non predictable events.

The programmable delays open the possibility for sending synchronous commands between BECs and GCUs. The cable and electronics delay mismatch compensation is mandatory; all the downstream and upstream delays have to be aligned toward the maximum latency in the system.

Clock alignment 1588 PTP over synch links



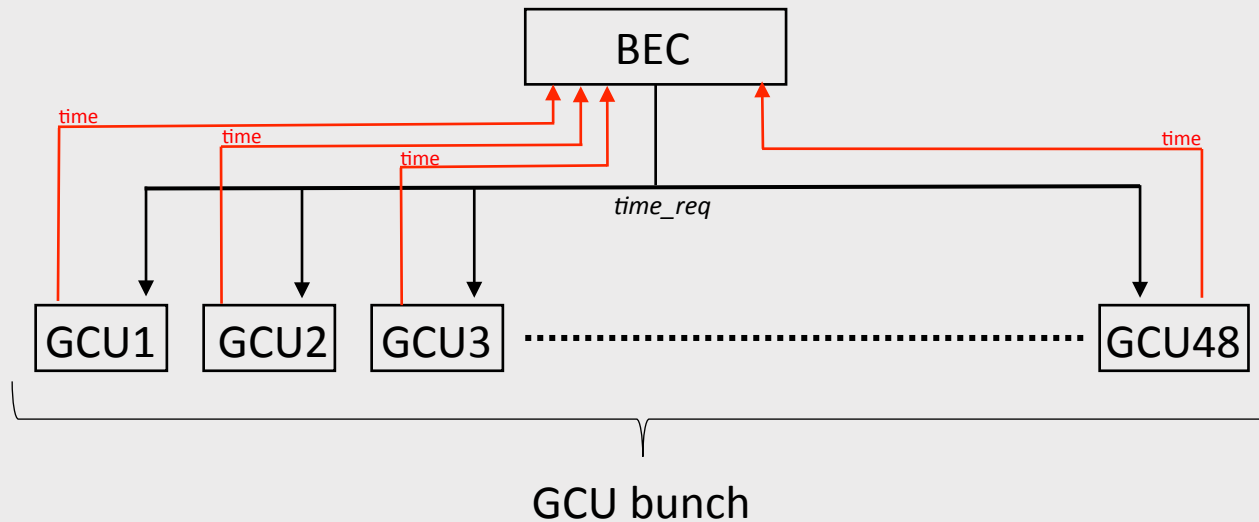
- $t1_g - t1_l = \text{clock offset}$ to be compensated
- At $t1_g$ BEC sends a synch message to GCU tagged with the BEC global time.
- GCU records the reception time $t2_l$.
- GCU computes $t1_g - t2_l = \text{clock offset} + \text{downstream delay}$.
- GCU sends a delay request message to BEC and records the transmission time $t3_l$.
- BEC records the reception time $t4_g$ and sends back a delay message tagged with $t4_g$.
- GCU computes $t4_g - t3_l = \text{upstream delay}$.
- Let's assume $t_diff = \text{downstream delay} - \text{upstream delay}$.
- t_diff is mainly due to the electronics delay mismatch between the downstream and upstream channels; **known** parameter.
- GCU can finally compute the offset:

$$\text{clock offset} = t1_g - t2_l - (t4_g - t3_l) - t_diff$$

This procedure, arbitrarily started by BEC must be repeated periodically and does not require the stop of data acquisition and generation of trigger requests. Indeed these synchronization messages can be sent among trigger requests and validations; $t3_l - t2_l$ and $t5_g - t4_g$ latencies are allowed to be non-deterministic since the important timestamp information is attached with the messages.

Clock Alignment Control

BEC card must periodically monitor the clock alignment status of the whole GCU bunch and eventually individually repeat the synchronization procedure and/or stop the data acquisition of a GCU resulting non-synchronized.



All the downstream channels have the same latency therefore all the GCUs receive *time_req* message at the same instant.

- BEC broadcasts the *time_req* command to all the GCU belonging to the bunch.
- Each GCU records the reception time and sends upstream the timestamp:

start	0	1	0	0	D	D	D	D	P	stop
-------	---	---	---	---	---	---	---	---	---	------

- The time information is encoded in several frames (4 bits each frame) depending on the number of bit of the local time counter (**open point**).
- BEC checks if the timestamps are aligned within 16 ns. If a GCU loses the synchronization it must be asked to stop the data acquisition and trigger request generation until a new alignment procedure has been successfully performed.
- This alignment check can be done runtime without stopping the data acquisition.
- BEC has the possibility to start and stop the data acquisition and subsequent trigger request generation via synchronous links using both broadcast commands or individual addressed commands.

Example : Test Pulse

- The test pulse is an example of predictable synchronous operation.
- Each GCU should start the test pulse generation at a well defined time.
- It is an important test for calibration, electronics monitor and TRG training.
- There will be a register reserved for the test pulse in the GCU configuration space. Via slow control sw can write this register with the time value at which the operation have to be executed.
- All GCU may be programmed to generate the test pulse at the same time.
- Or SW can program the BEC to broadcast the test pulse command to all the GCU belonging to that bunch at a preset time.

Local Clock Reset and Event Counter Reset

- The local time counter reset operation is synchronous; even for this operation is not possible to send a synchronous reset message from the CTS to all the GCUs but instead CTS, BECs and GCUs must all be programmed to auto-generate a synchronous internal reset at a pre-programmed time t_{reset} .
- The local clock reset can be used to prevent the time counter overflow.
- The event counter reset operation is another example of predictable synchronous operation. The BEC card can broadcast the event counter reset command to all the GCU belonging to that bunch via TTC system.

GCU Firmware Schedule

- End 2016 - Q1/2017: prototype firmware for hardware test
 - FMC, **ADC I/F**
 - DDR3
 - Cable drivers/receivers + power, HV I/F
 - Ethernet
 - CPLD
 - CDR
- Q2 2017 : deployment firmware V. 0.0
 - **Needs ASAP**
 - **ADCs (either Vulcan and Tsinghua)**
 - **BEC**
 - **Trigger “processor”**
 - **“Final” cable**
 - **Power Board**
 - **Prototype DAQ**