Backend Card status

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outlines

- Current layout
- V2 Prototype
- Test results
- Future plan
- Open question

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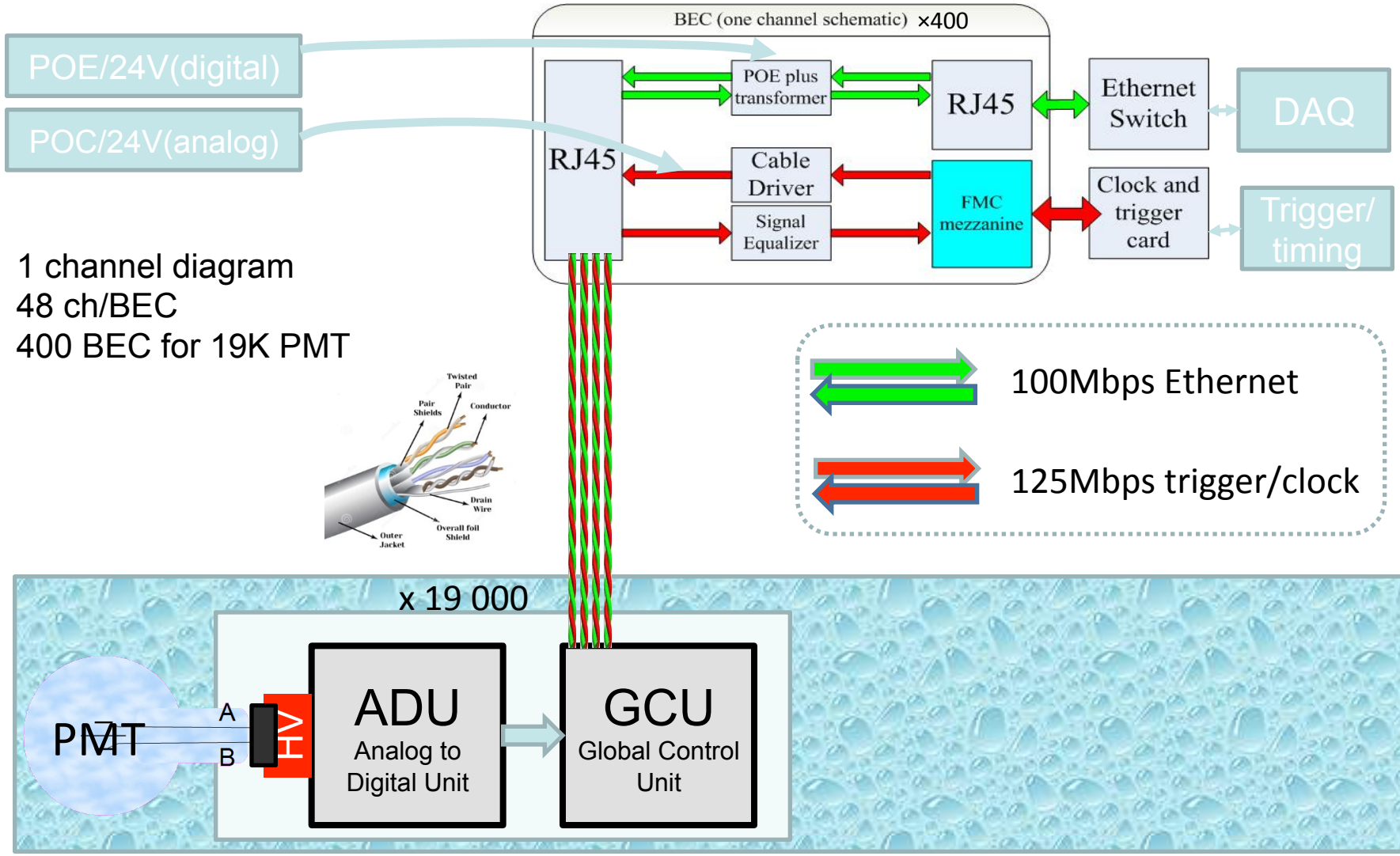
JUNO electronics system



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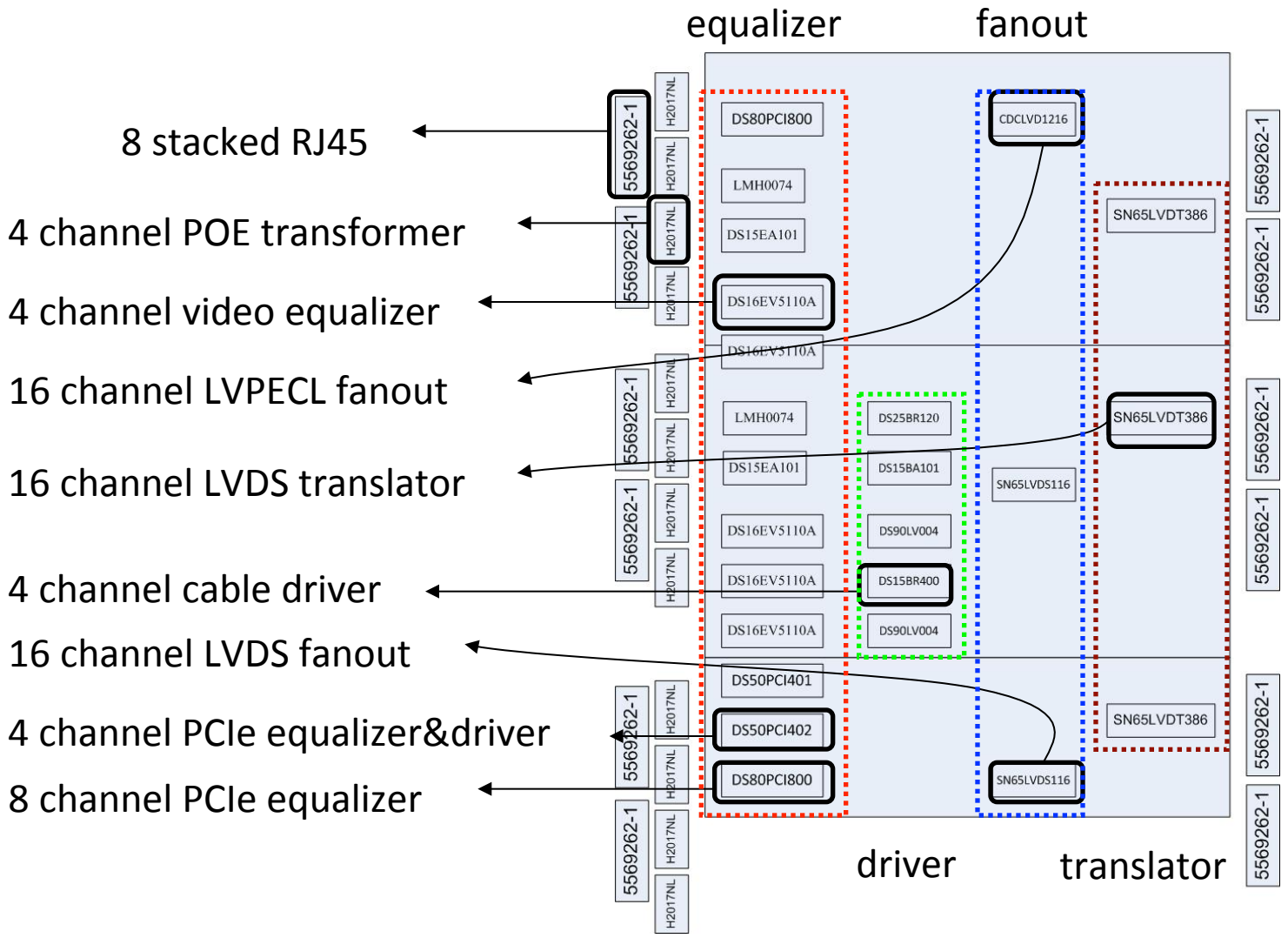
V2 Prototype

- Why ?
- Gain experience of 48 channels integration
- Better understanding of schedule and cost
- Test platform for multiple configuration
- Try interface to different system
- Find best equalizer/driver combination for different requirements (swing, jitter, crosstalk…)
- How ?
- Build 48 channel with different combination
- Do not take special care of power supply and isolating

V2 Prototype

- Equalizer
- Single channel
- Multi-channel
- Video Oriented(4 channel)
- PCIe Oriented(4 or 8 channel)
- Driver
- Different swing
- LVDS
- LVPECL
- ADJ
- Different shape
- With pre-emphasis

V2 Prototype



V2 Prototype

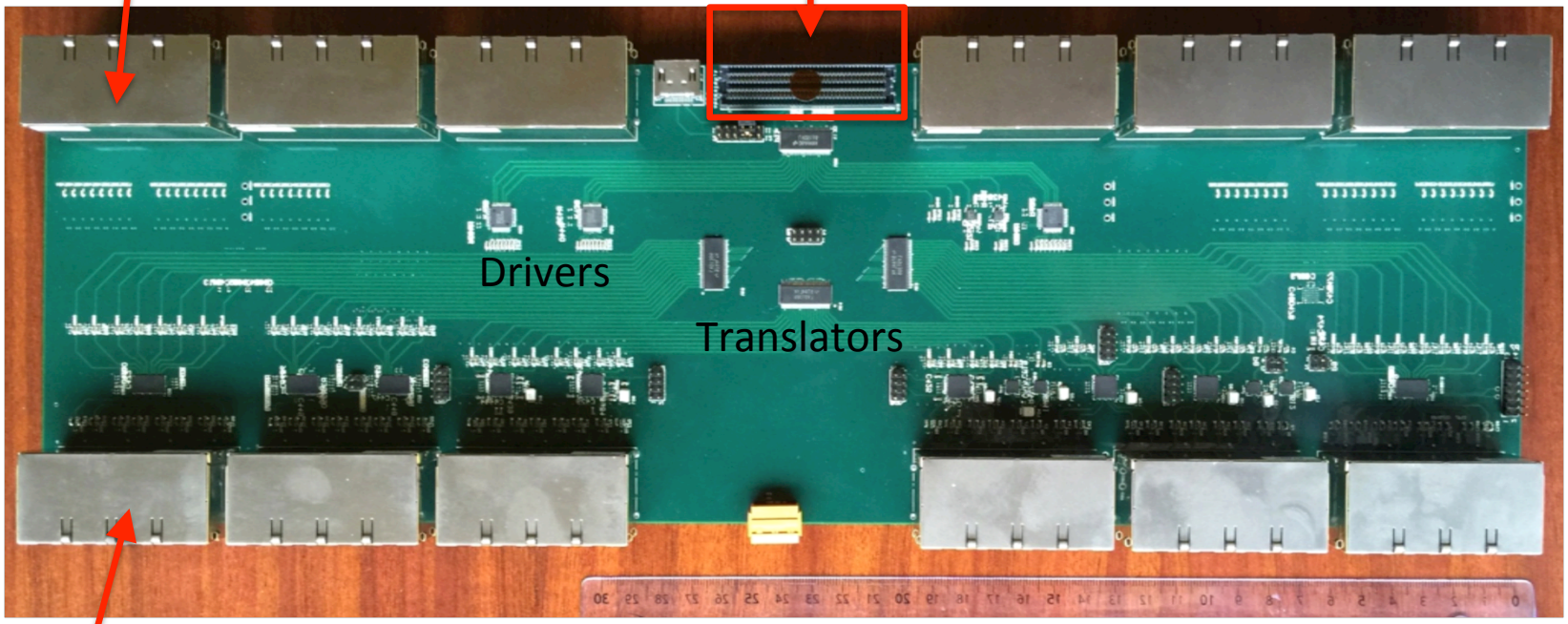
DAQ

Trigger/Clock/DCS

8 layer PCB
48 cm x15 cm

8 Ethernet connectors (RJ45)

FMC connector



Equalizers

8 Ethernet connectors

GCU

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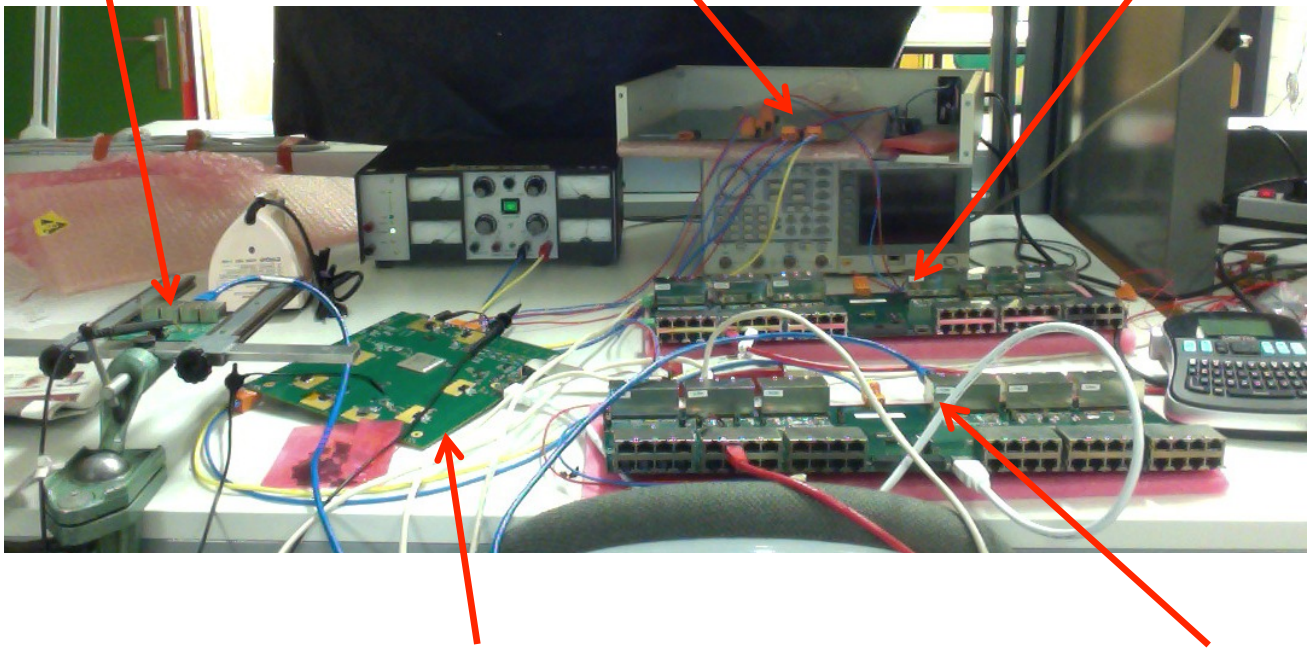
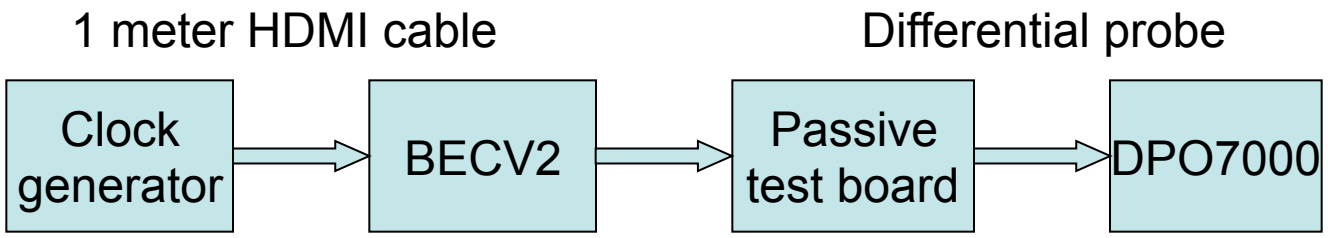
Test setup


Passive test board
Power supply board
BECV2_02(receiver)
Clock generator board
BECV2_01(transmitter)

Test steps

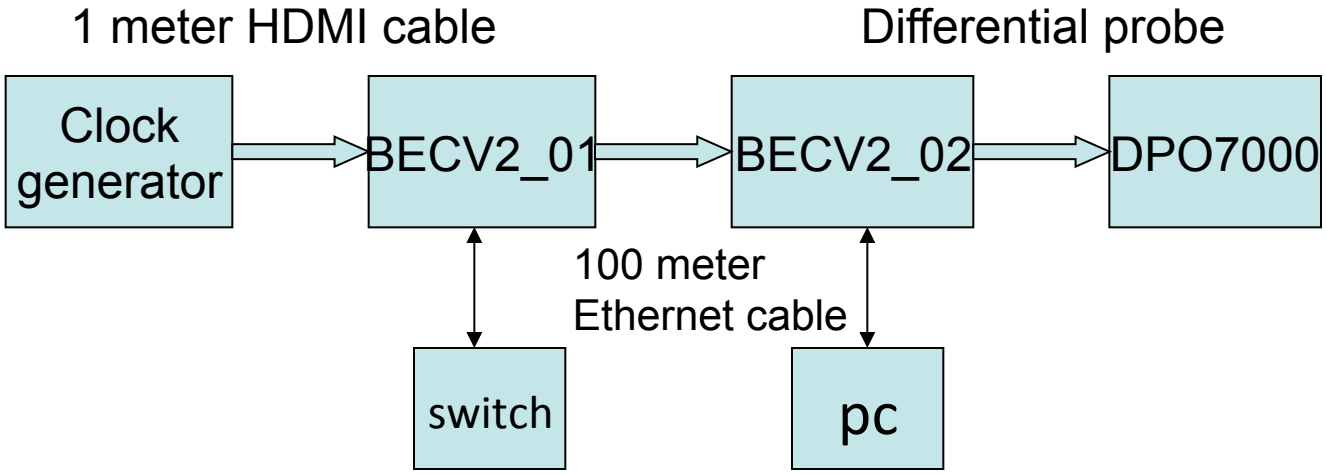
- Signal source test
- Equalizer test
- Ethernet test
- Power injection test
- All in one test

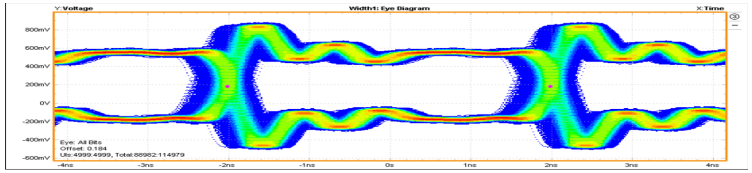
Signal source test

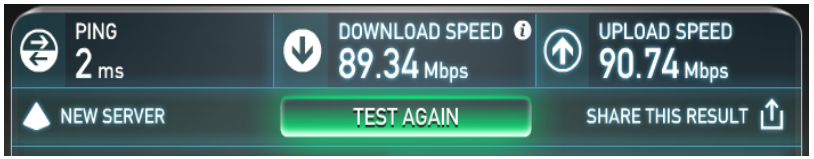


	2 meter Ethernet cable	
	125MHz	250MHz
Lvds fanout	20ps/0.8v	32ps/1.1v
Lvpecl fanout	25ps/2.3v	27ps/2.5v

Single channel chip test





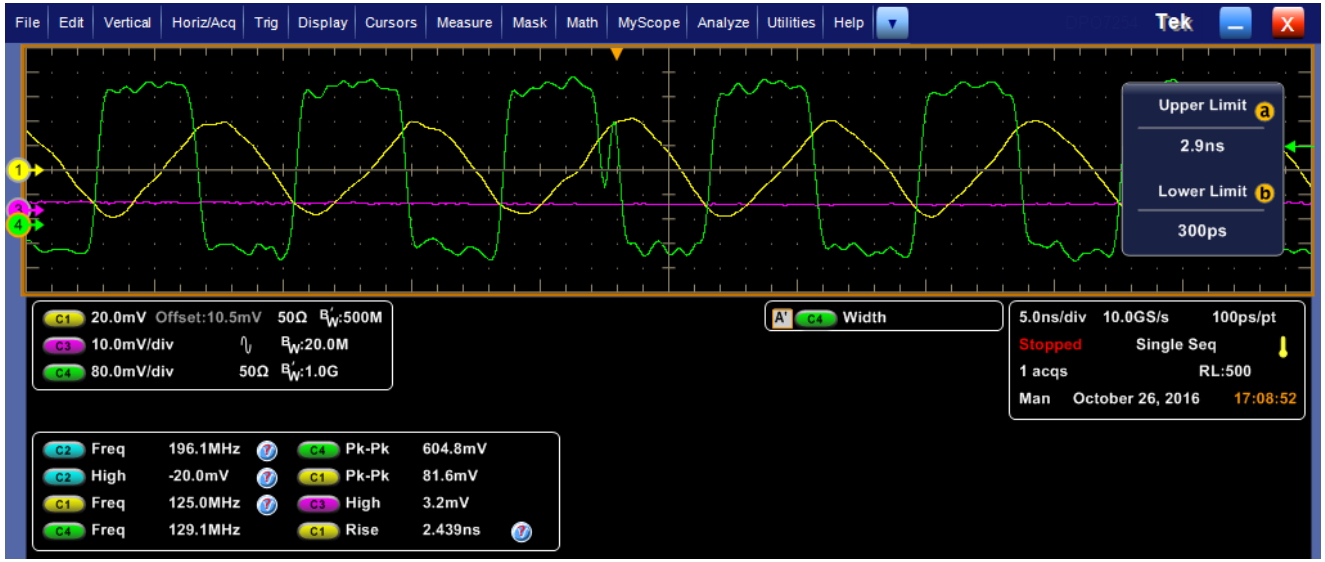


Equalizer/cable driver test :
Equalizer: DS15EA101
Driver: LVPECL
Period std dev : 115ps

Ethernet data test :
Transformer: H2017NL- with POE 30V

Multi-channel chip test

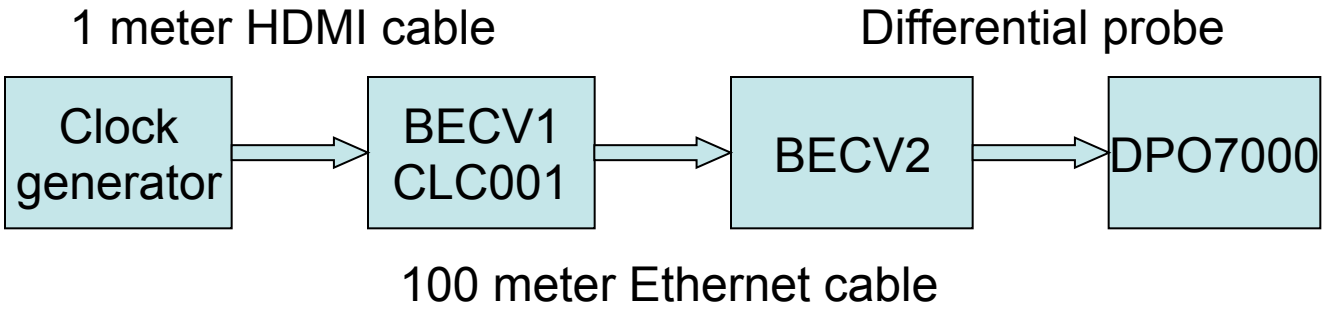
	50 meter		100 meter		
	125MHz	250MHz	62.5MHz	125MHz	250MHz
Lvds fanout	56ps/0.6v	50ps/0.6v	glitch	glitch	glitch
Lvpecl fanout	55ps/0.6v	56ps/0.6v	92ps/0.6v	112ps/0.6v glitch	glitch



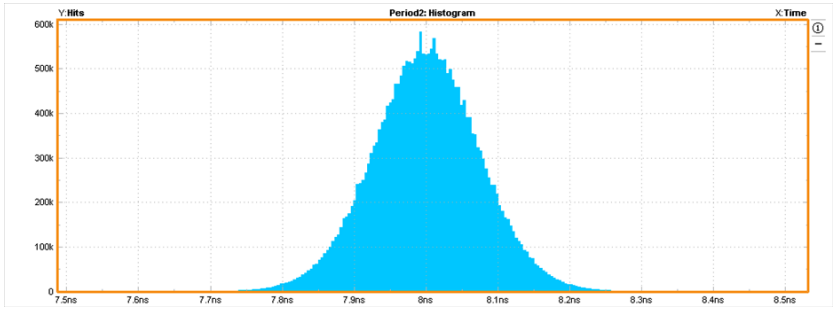
Equalizer:DS16EV5110A

Glitch: Maximum 500ps, may not affect data transfer, need further study

Multi-channel chip test



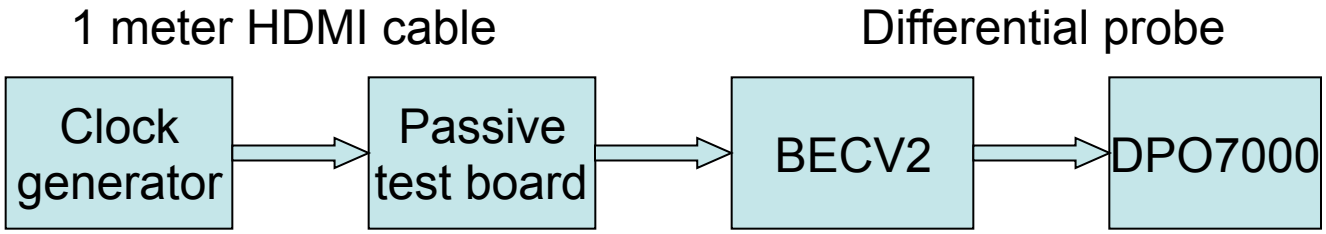
swing	jitter
1v	glitch
2.5v	91ps



Period std dev : 75ps

Glitch may related to input signal swing

FPGA direct drive test



	2 meter		50 meter		100 meter		
	125MHz	250MHz	125MHz	250MHz	62.5MHz	125MHz	250MHz
Lvds	30ps/1.3v	30ps/1.4v	75ps/0.6	60ps/0.6v	glitch	glitch	glitch
Single lvcmos	14ps/2.2v	27ps/2.8v	27ps/0.6v	40ps/0.6v	87ps/0.6v	112ps/0.6v glitch	113ps/0.6v glitch
Double lvcmos	16ps/5.1v	20ps/6.0v	24ps/0.6v	28ps/0.6v	49ps/0.6v	63ps/0.6v	56ps/0.6v

Pseudo differential output is more stable and flexible

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Future plan

- Combine test with Aachen about power delivery
- Repeat test with real cable
- Start V3 design

To be fixed before V3 design

- Decide equalizer and cable driver
- Decide current on PCB wire
- Decide POE and POC grouping
- Can we use two POC rather than one ?

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Open question

- Grounding and shielding
- Cable length
- Acceptance specification
- Mass production and quality control

Thank you!

Single channel test

- Driver: LVDS fanout
- Cable: 100 meter
- 125000 cycle per measurement for more then 24 hours