The JUNO Experiment

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Outlines

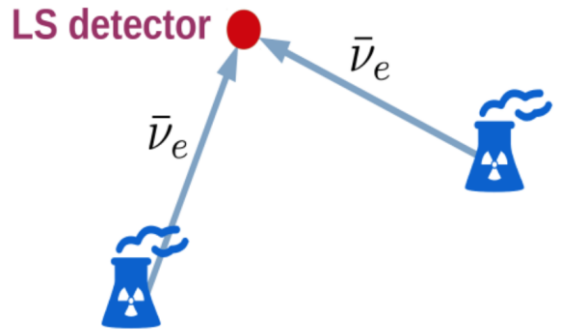
- The JUNO experiment
- The IIHE JUNO team and activities
- Progress of backend card in 2019

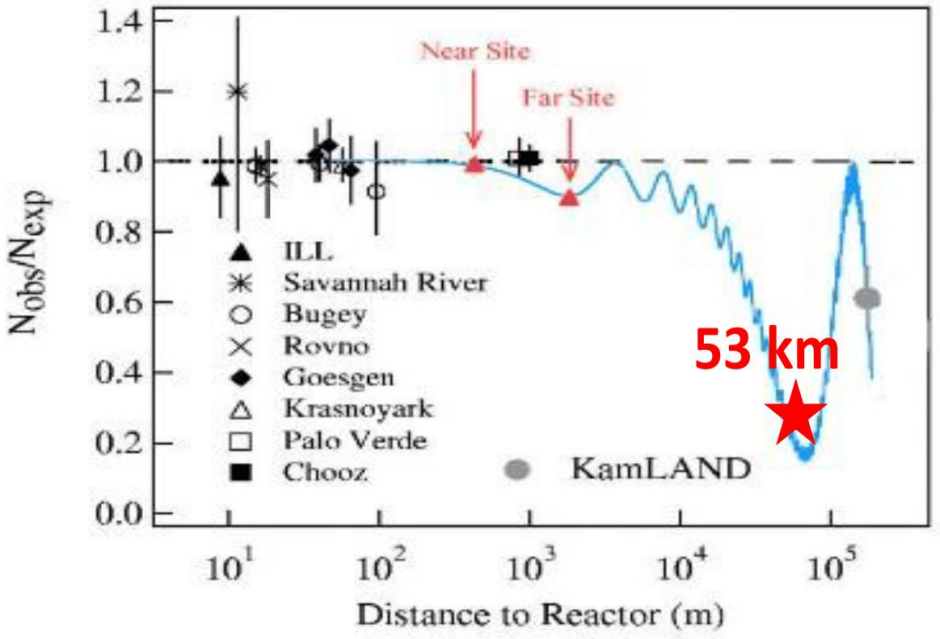
The JUNO experiment

The JUNO project

- JUNO = Jiangmen Underground Neutrino Observatory
- JUNO is a “medium-baseline” (53 km) reactor neutrino experiment

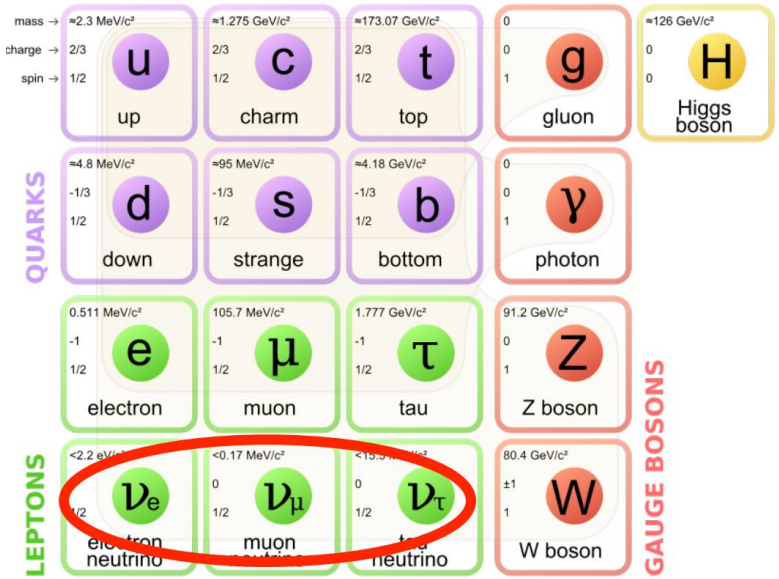
  located in China

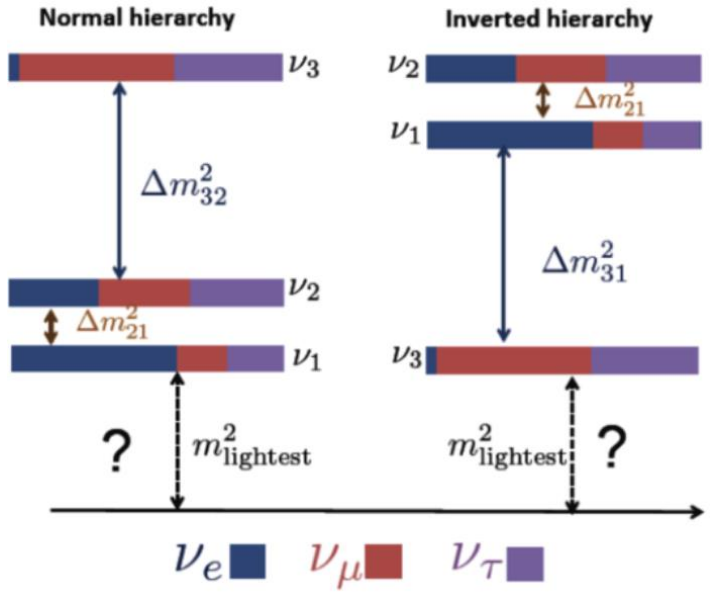




Cores	YJ-C1	YJ-C2	YJ-C3	YJ-C4	YJ-C5	YJ-C6
Power (GW)	2.9	2.9	2.9	2.9	2.9	2.9
Baseline (km)	52.75	52.84	52.42	52.51	52.12	52.21
Cores	TS-C1	TS-C2	TS-C3	TS-C4	DYB	HZ
Power (GW)	4.6	4.6	4.6	4.6	17.4	17.4
Baseline (km)	52.76	52.63	52.32	52.20	215	265

The JUNO project





Parameter	Current precision	JUNO goal
$Sin^2 2\theta_{12}$	6%	0.7%
Δm^2_{12}	3%	0.6%
$\lvert\Delta m^2_{32}\rvert$	5%	0.5%
MH	N/A	3-4σ
$sin^2 2\theta_{13}$	3%	15%

Study of the neutrino particles …

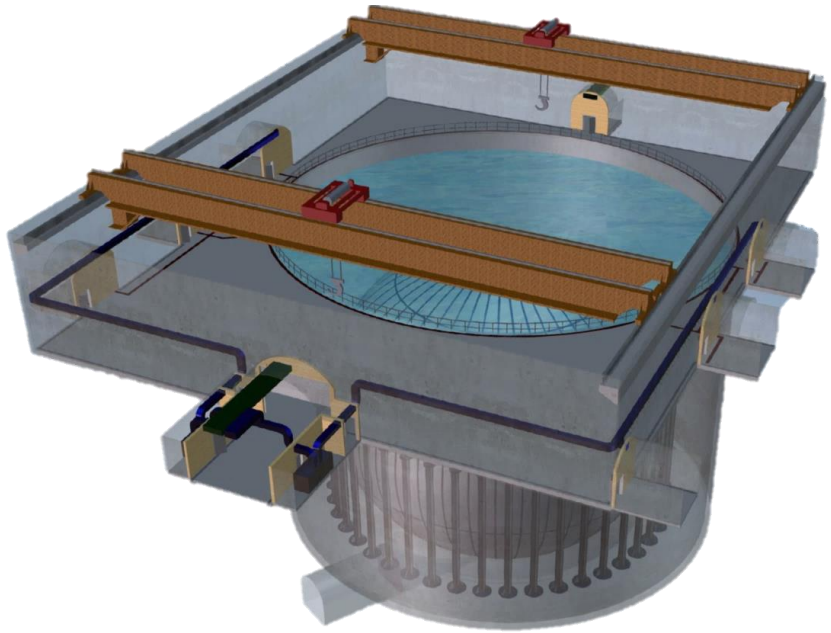
(nearly massless, very weakly interacting)

- Determine the neutrino mass hierarchy (NMH)
- Measure oscillation parameters

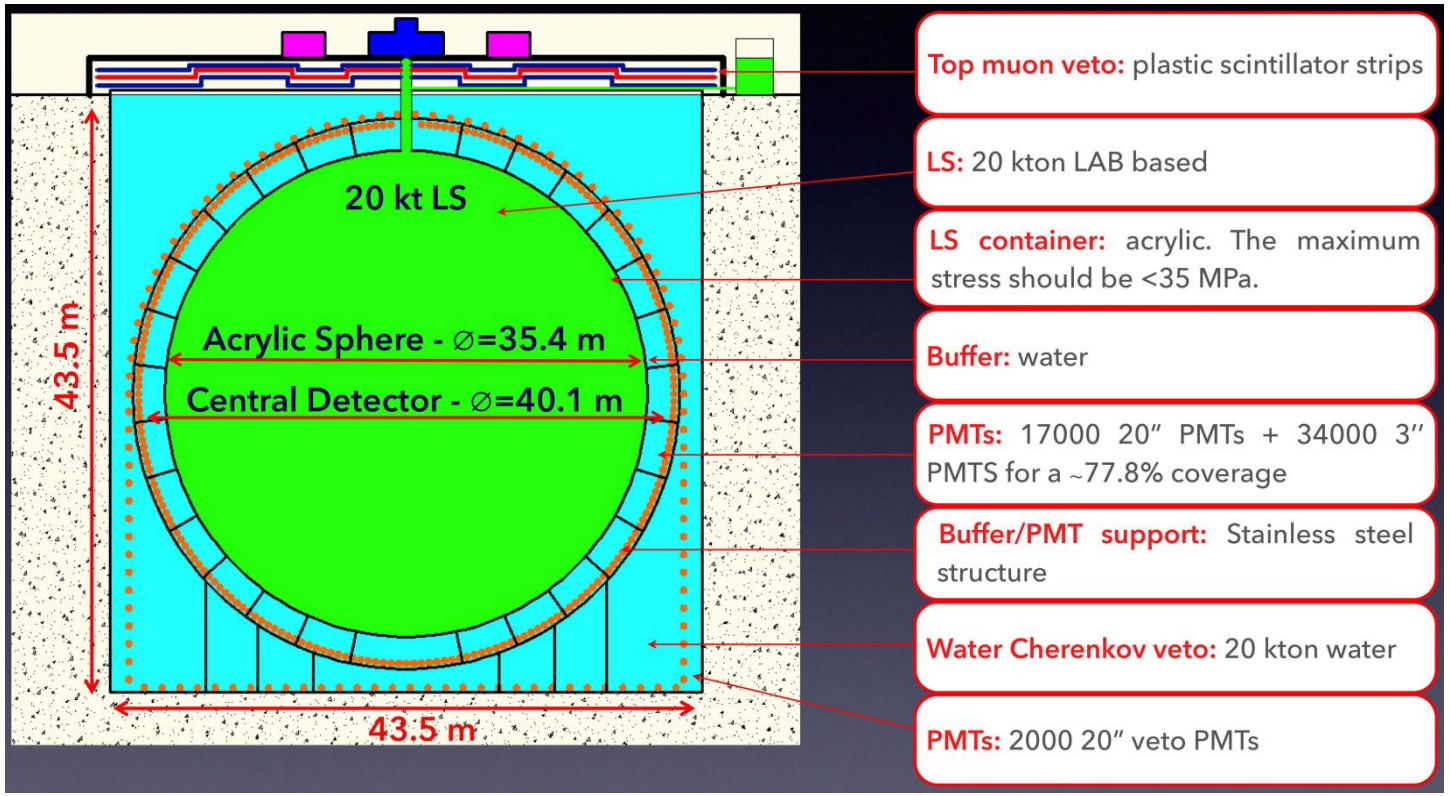
But also :

- Neutrino from supernova burst
- Solar neutrinos
- atmospheric neutrinos
- Geoneutrinos
- Exotic searches as nucleon decay and dark matter…

The JUNO detector



Photomultiplier tube (PMT)



Neutrinos are observed via
Inverse Beta Decay (IBD) :

$$\bar{\nu}_e + p \rightarrow e^+ + n$$

$$\tau \simeq 200\mu\text{sec} \rightarrow n + p \rightarrow d + \gamma$$

Experiment	Daya Bay	BOREXINO	KamLAND	JUNO
LS mass	20 ton	~ 300 ton	~ 1 kton	20 kton
Coverage	~ 12%	~ 34%	~ 34%	~ 80%
Energy resolution	~ 7.5%/$\sqrt{E}$	~ 5%/$\sqrt{E}$	~6%/$\sqrt{E}$	~3%/$\sqrt{E}$

JUNO construction status

Experimental Hall is only 1.5 m short to the final top arc structure.

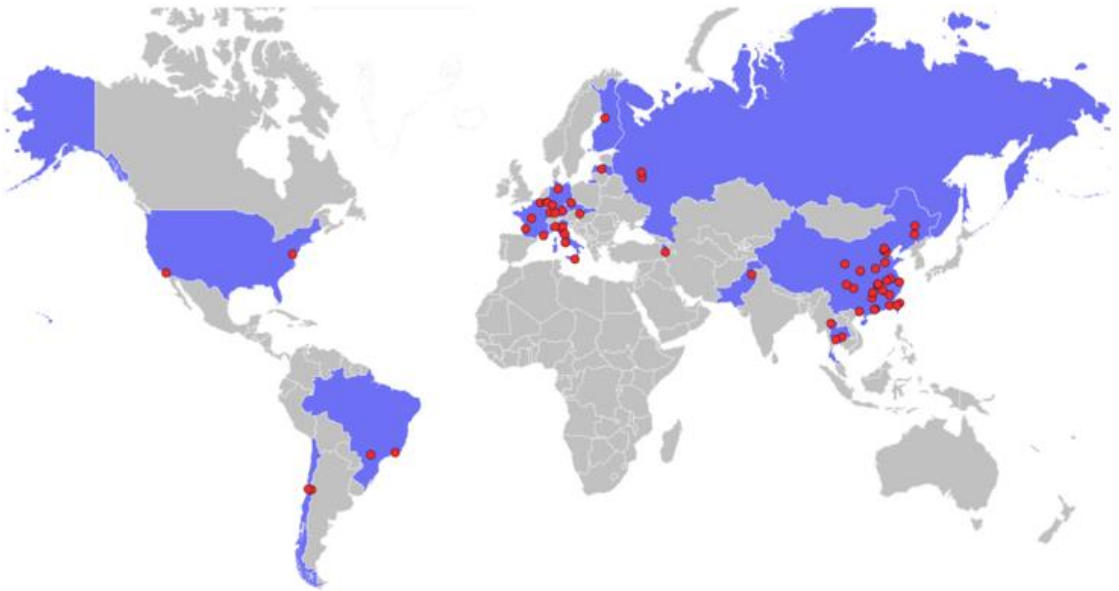
Schedule:

- Surface buildings will be completed at end of 2019
- The experimental hall will be completed on 2020.6.30

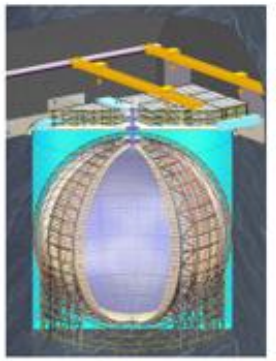
JUNO collaborators

Now : 77 institutes

About 600 members



JUNO timeline



2014:

- International collaboration established

2015:

- PMT production line setup
- CD parts R&D
- Start civil construction

2016:

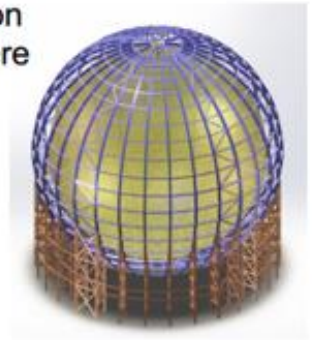
- Start PMT production
- Start CD parts production

2017:

- Start PMT testing
- TT arrived

2018 - 2019:

- PMT potting starts
- Delivery of surface buildings
- Start production of acrylic sphere

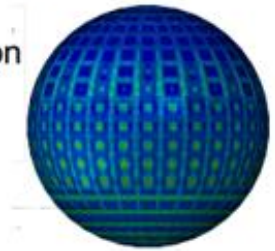


2020 - 2021

- Electronics production starts
- Civil work and lab preparation completed;
- Detector constructing

2022:

- Detector ready
- Data taking!



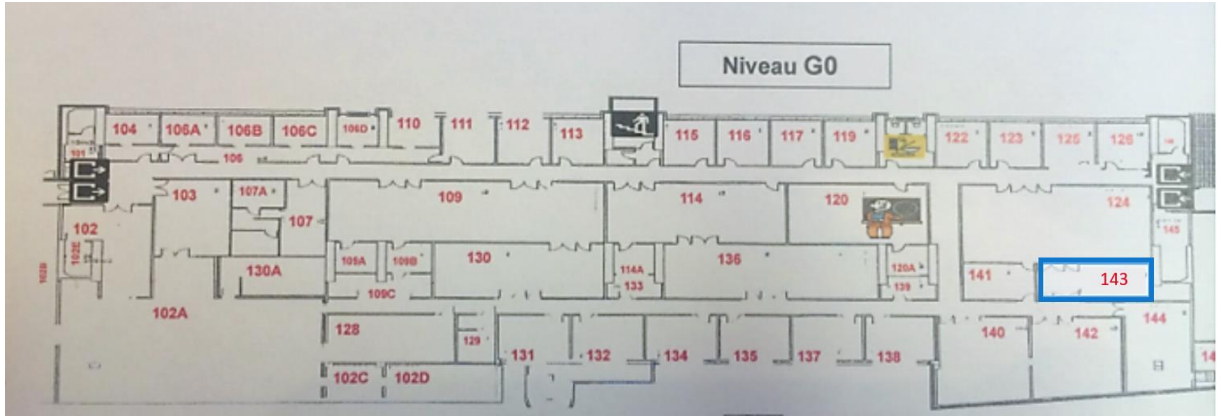
The IIHE JUNO team and activities

The IIHE JUNO team

The dream team :

- Barbara Clerbaux
- Yifan Yang
- Pierre-Alexandre Petitjean (PhD student)
- Shuang Hang (Visiting PhD student)
- Benoit Denègre

JUNO electronics lab: room 143



The IIHE JUNO activities

Main focus since 2016 :

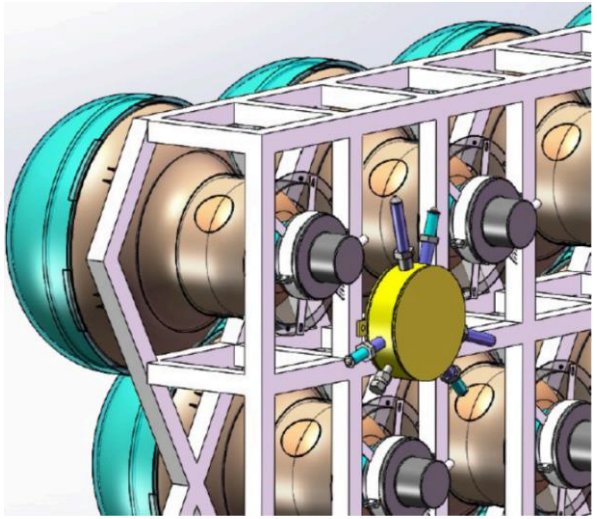
Design and test of the BEC (Back end cards) of the JUNO electronics system

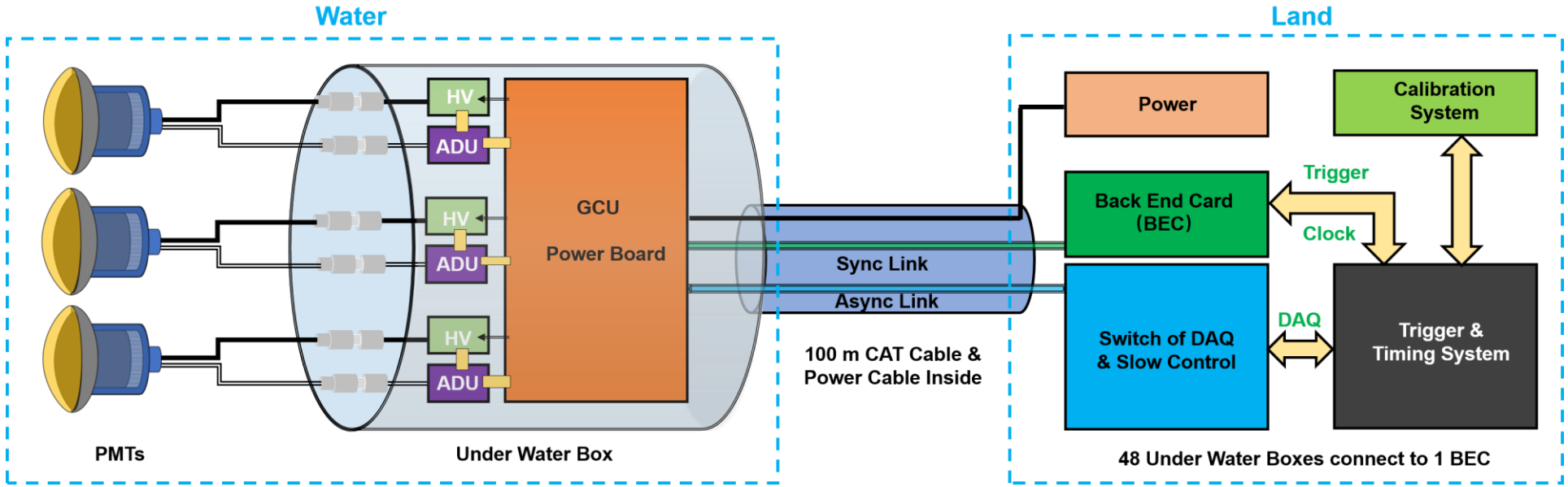
Activities in 2019：

- January to March: test of BEC v3.0
- April to June : design and short-term test of BEC v4.0
- July to November: long-term test of BEC v4.0

Progress of backend card in 2019

JUNO readout system and BEC overview





- PMT: photomultiplier tubes
- HV: High voltage units
- ADU: Analog to Digital Unit
- GCU: Global Control Unit
- CAT cable: Category 5e cable

- BEC will be used to link underwater system to trigger and clock system sitting outside water
- 48 GCU to 1 BEC, around 150 BEC are needed
- 48 100 meters cable to 1 BEC, 4 channels per cable

Latest design of BEC ▶ BEC v4.0

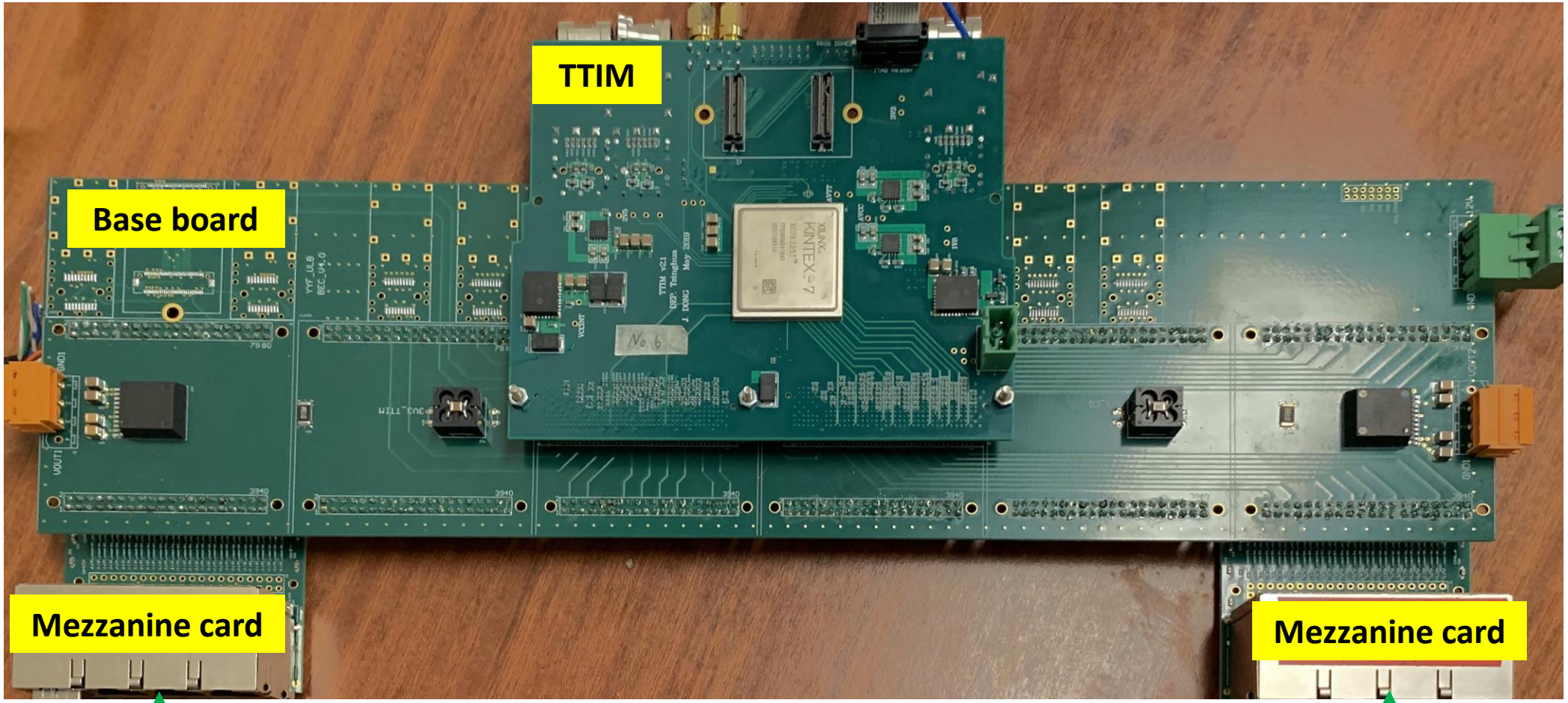
BEC v3.0

Channel	Signal	Direction	Current bandwidth
1, 2	Trigger accept + Clock	B2G	250 Mbps
3, 6	Trigger request + Slow control	G2B	250 Mbps
4, 5	Low Voltage Positive	-	-
7, 8	Low Voltage Negative	-	-

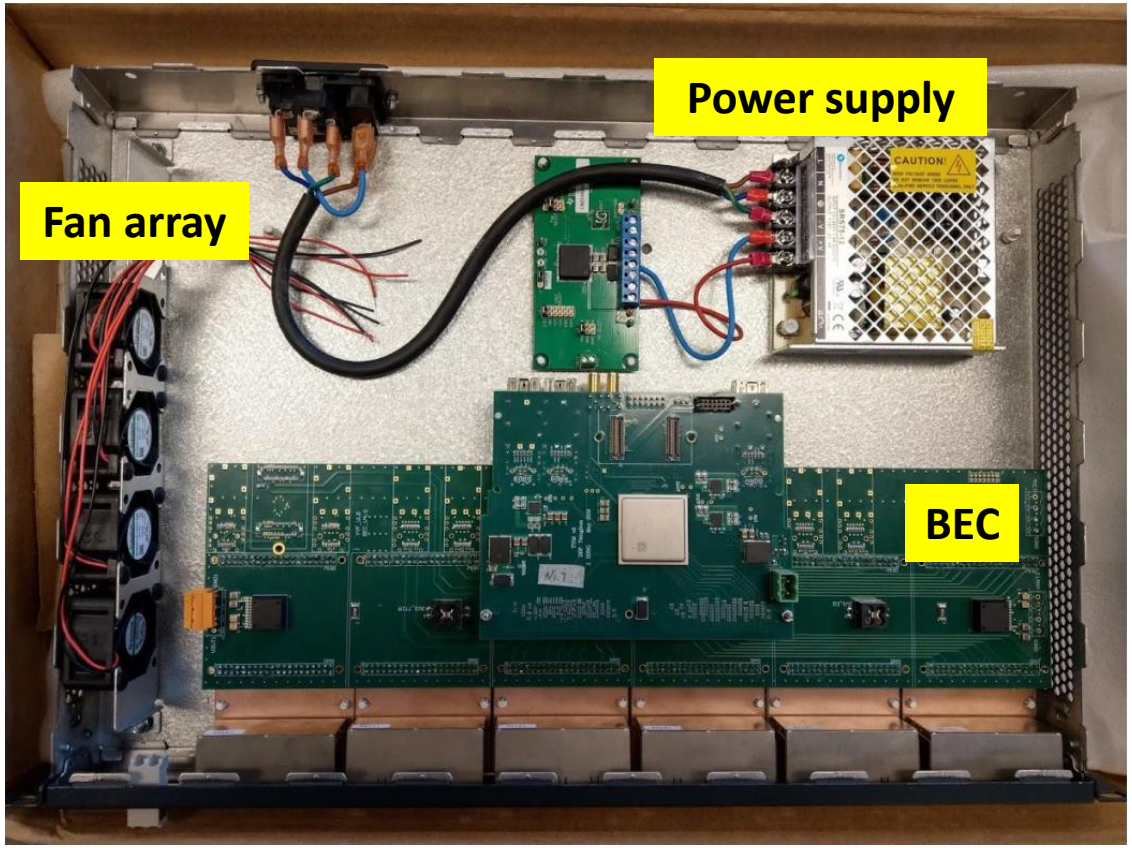
BEC v4.0

Channel	Signal	Direction	Error tolerance	ECC	Current bandwidth
1, 2	Clock	B2G	No	No	62.5 MHz
3, 6	Trigger accept	B2G	No	Yes	125 Mbps
4, 5	Trigger request	G2B	Yes	No	125 Mbps
7, 8	Slow control	G2B	Yes	Yes	125 Mbps

Latest design of BEC ▶ BEC v4.0



Latest design of BEC ▶ BEC v4.0



- Based on nVent-Schroff 1U 19-Inch Wall Cabinet 44×444×310 mm
- Special thanks to Benoît.

Test result

One board test:

- Short term test： eye diagram and bathtub curve
- Long term test： 72-hour bit error rate test

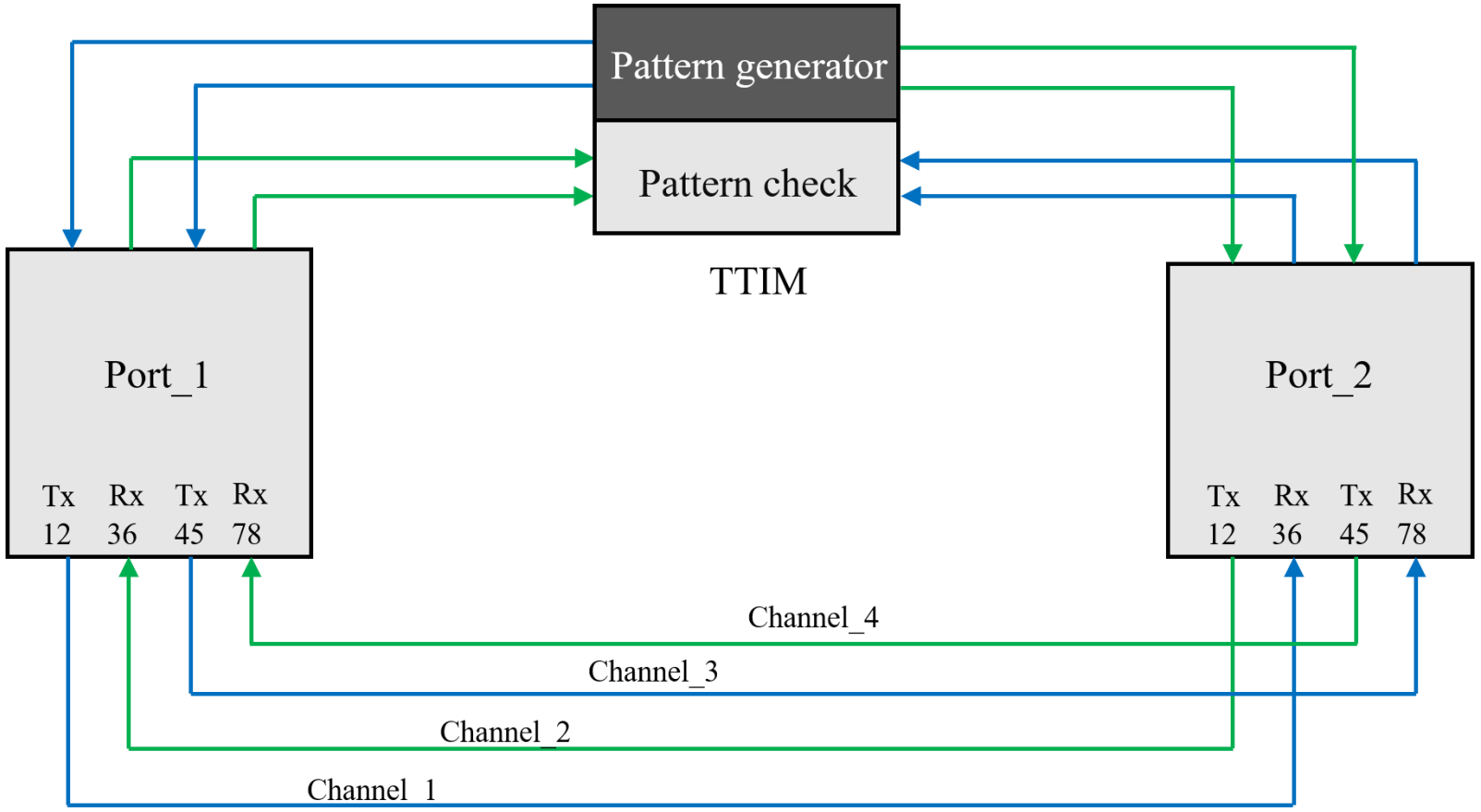
Two boards test:

- Long term test： 3 times 72-hour bit error rate tests

Combined test:

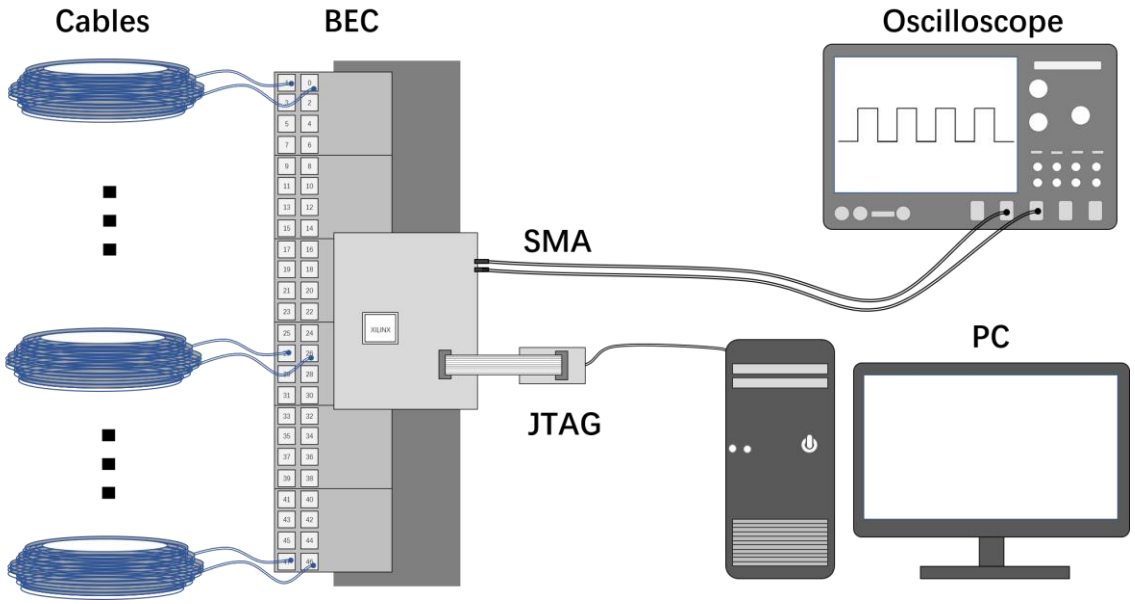
- In Padova
- In Beijing

One board test

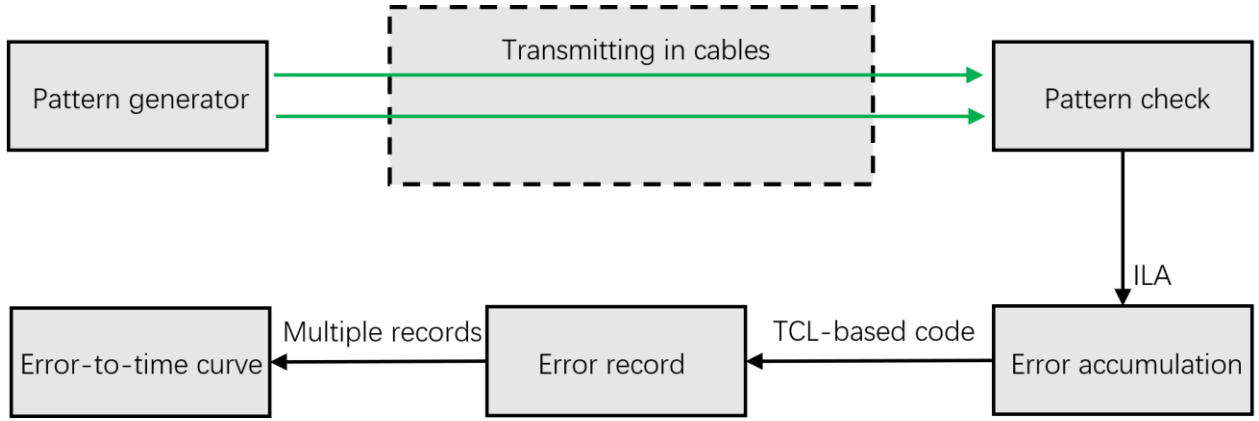


Multi-channel closed-loop diagram of one board test

One board test ▶ Automatic test plan



Automatic test plan for one board test

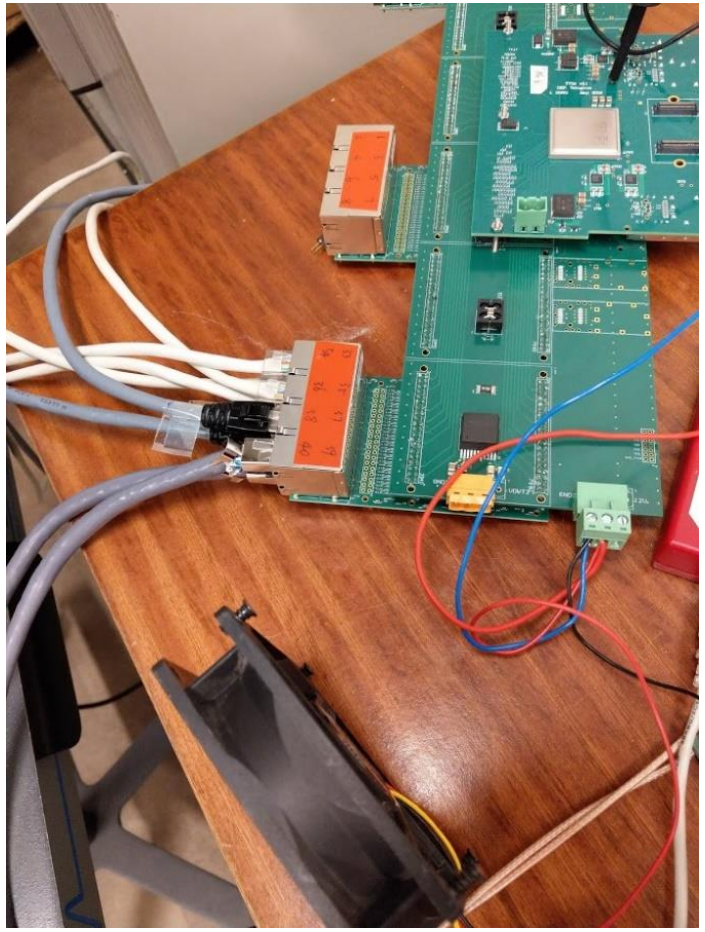


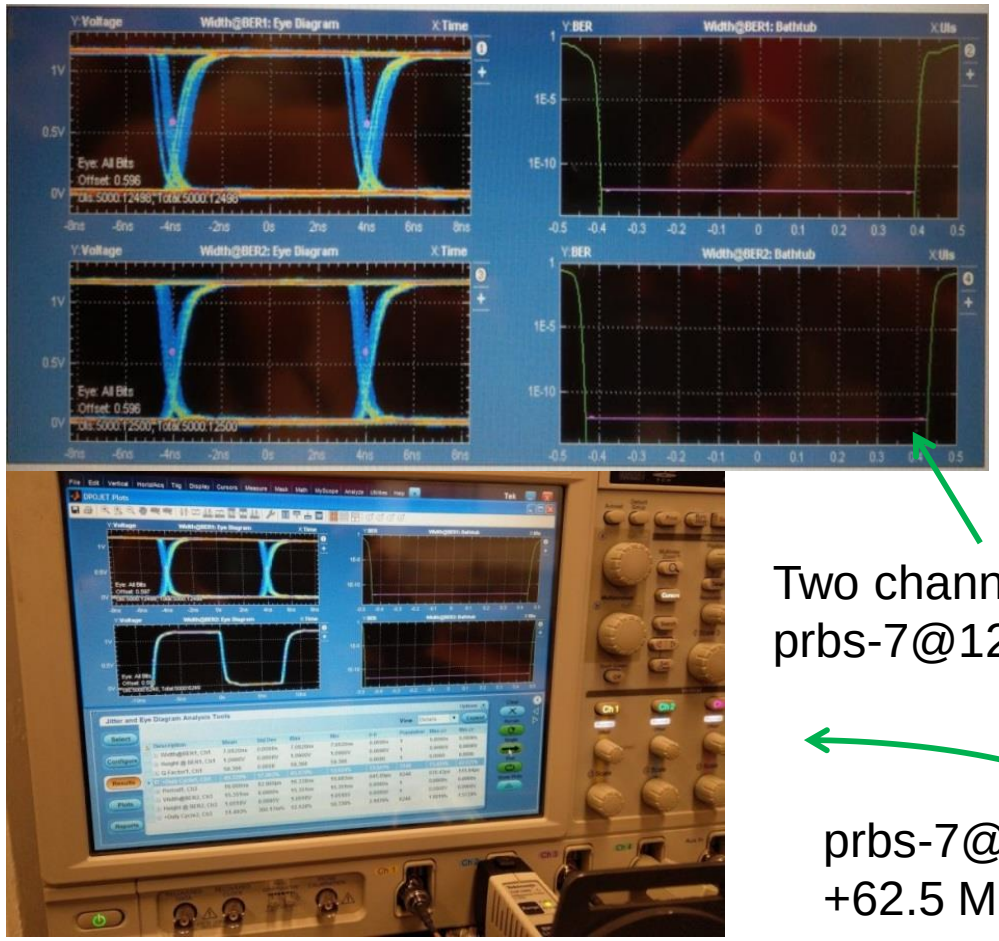
Automatic test process

Material needed:

Cat5e FTP cables; 2 Small A Type (SMA) cable; 1Joint Test Action Group (JTAG) Cable; 1 PC with vivado 2018.1; 1 oscilloscope with eye diagram.

One board test ▶ Short term test





Two channels
prbs-7@125 Mbps

prbs-7@125 Mbps
+62.5 MHz

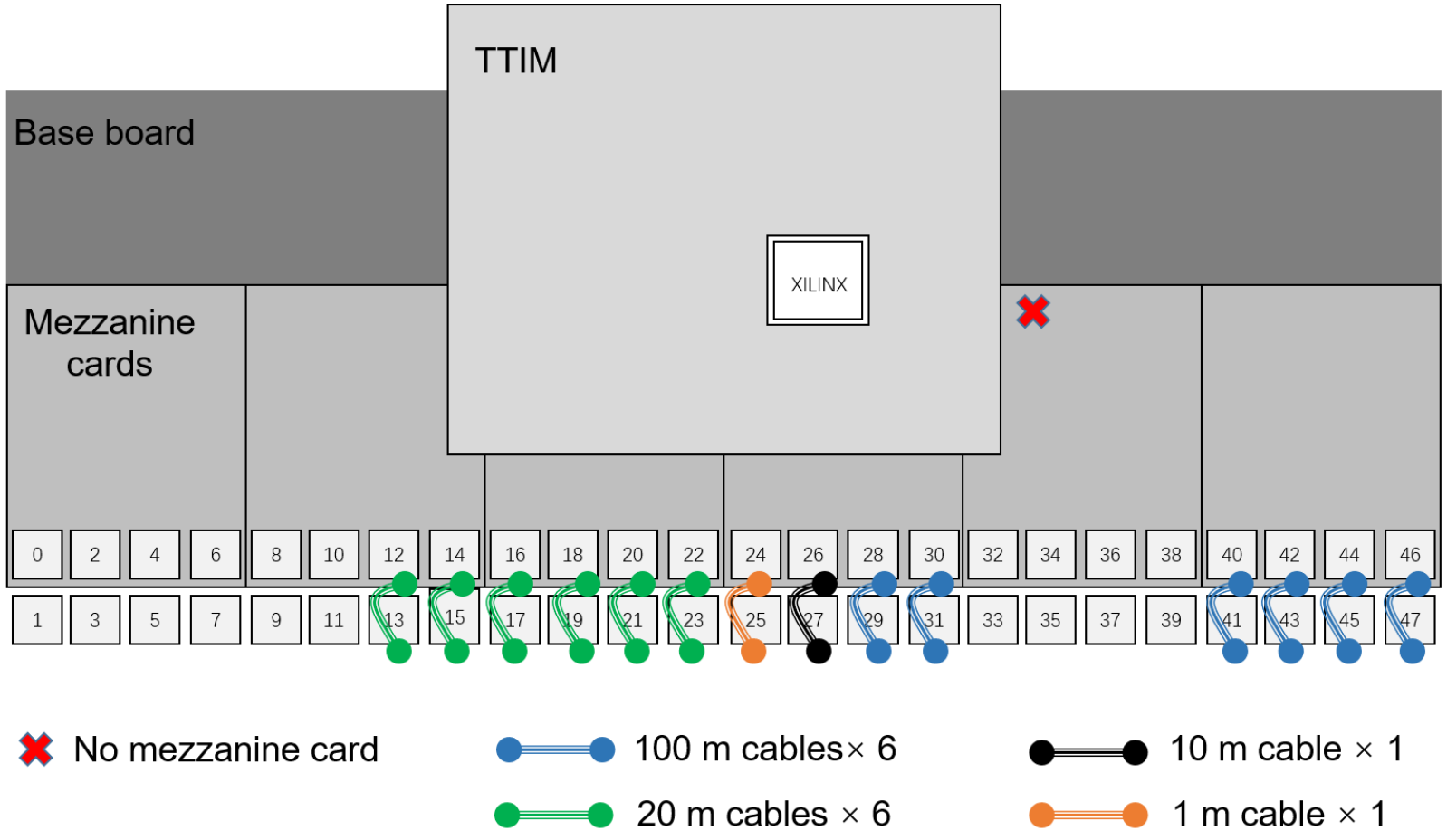
- Pseudo-Random Binary Sequence-7 (PRBS-7)@125 Mbps was transmitted.
- Eye diagram: created by superimposing successive waveforms to recognize signals distortion.
- Bathtub curve: display the interval that can be used for sampling.

One board test ▶ Long term test

Port1	Port2
1-2 (prbs)	3-6 (checker)
3-6 (checker)	1-2 (prbs)
4-5 (prbs)	7-8
7-8	4-5 (prbs)

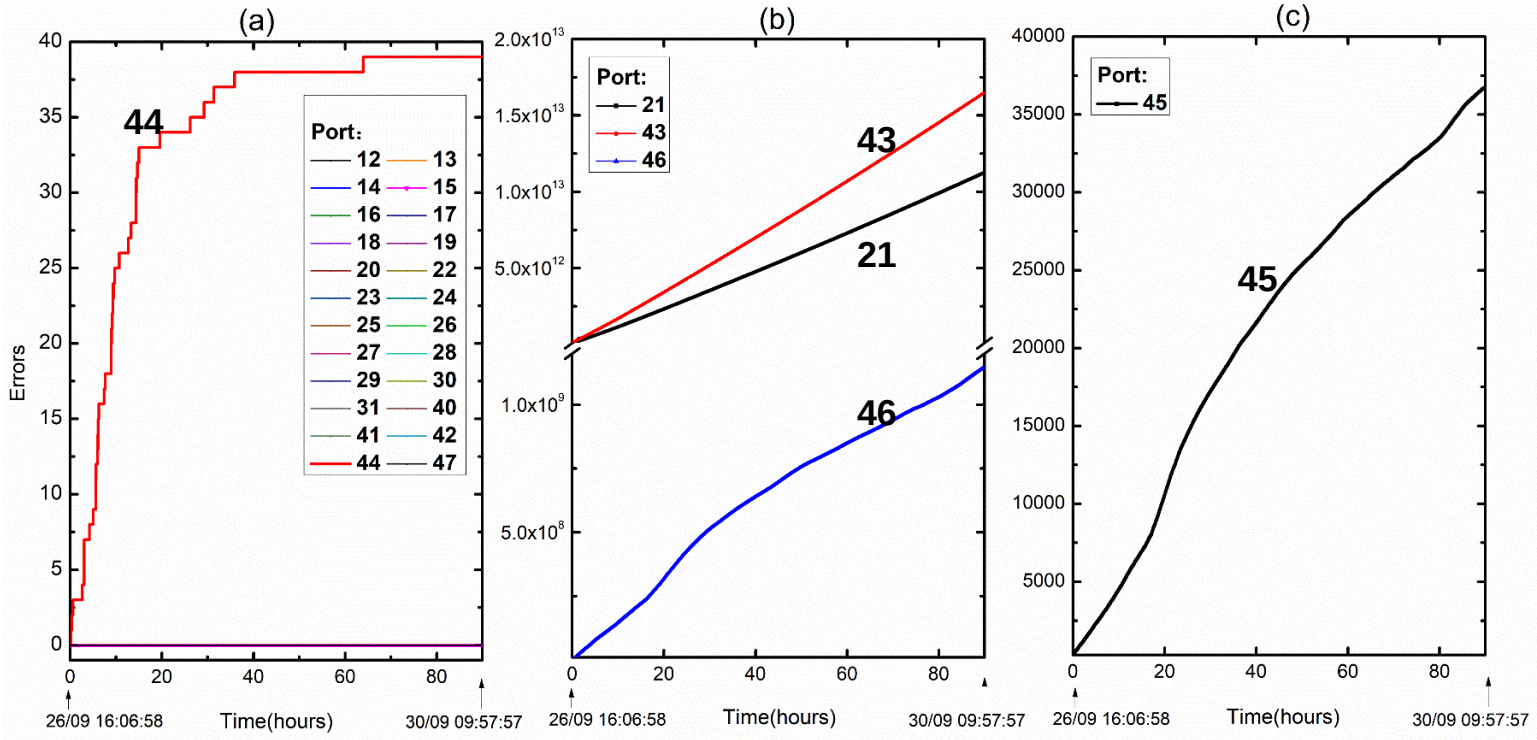
- 90 h continuous test
- 14 cables work simultaneously
- 4 channels per cable
- Prbs-7@250 Mbps per channel

One board test ▶ Connection plan



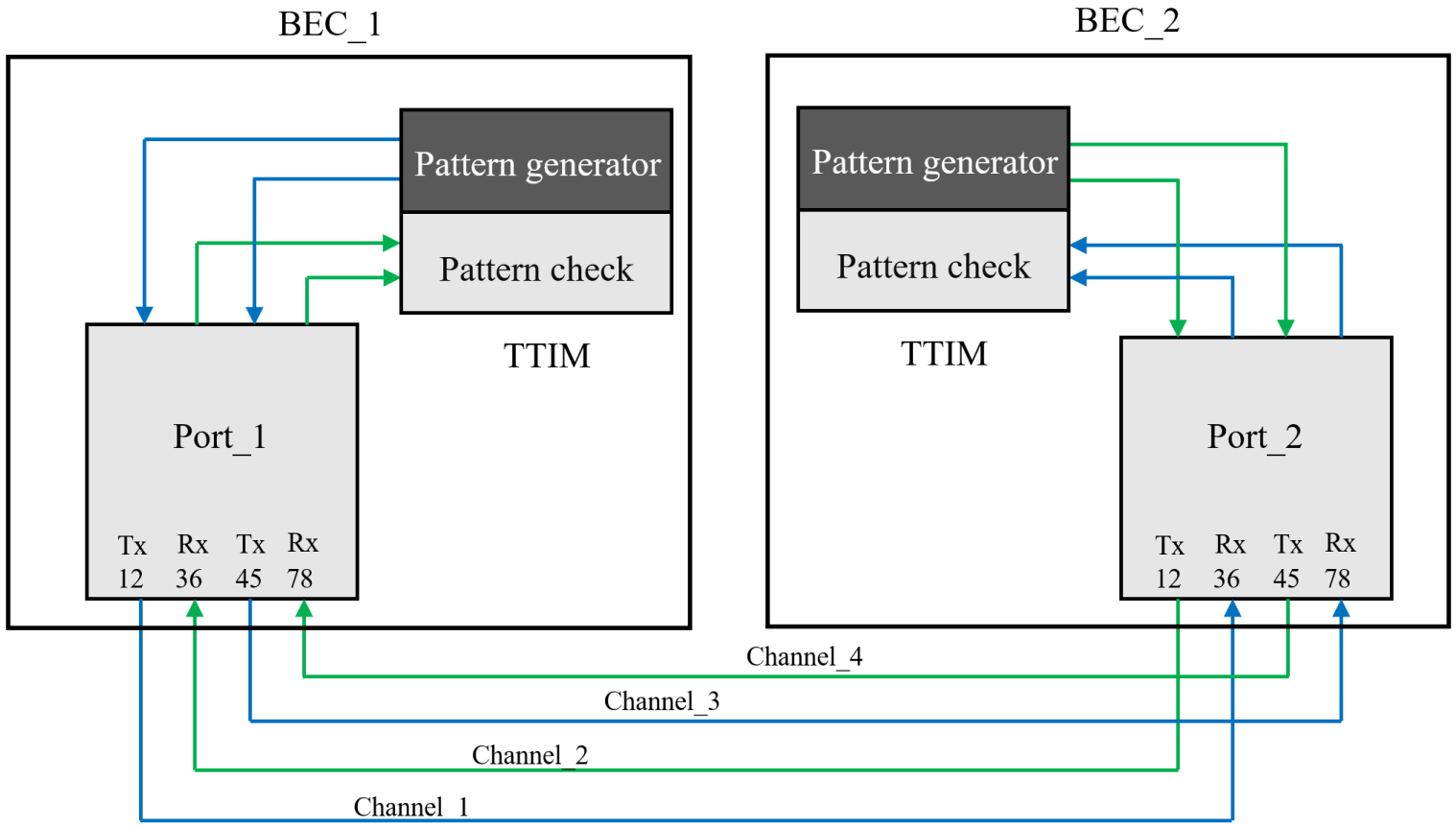
One board test ▶ PRBS error check

PRBS error check for 28 channels (always check 3_6)



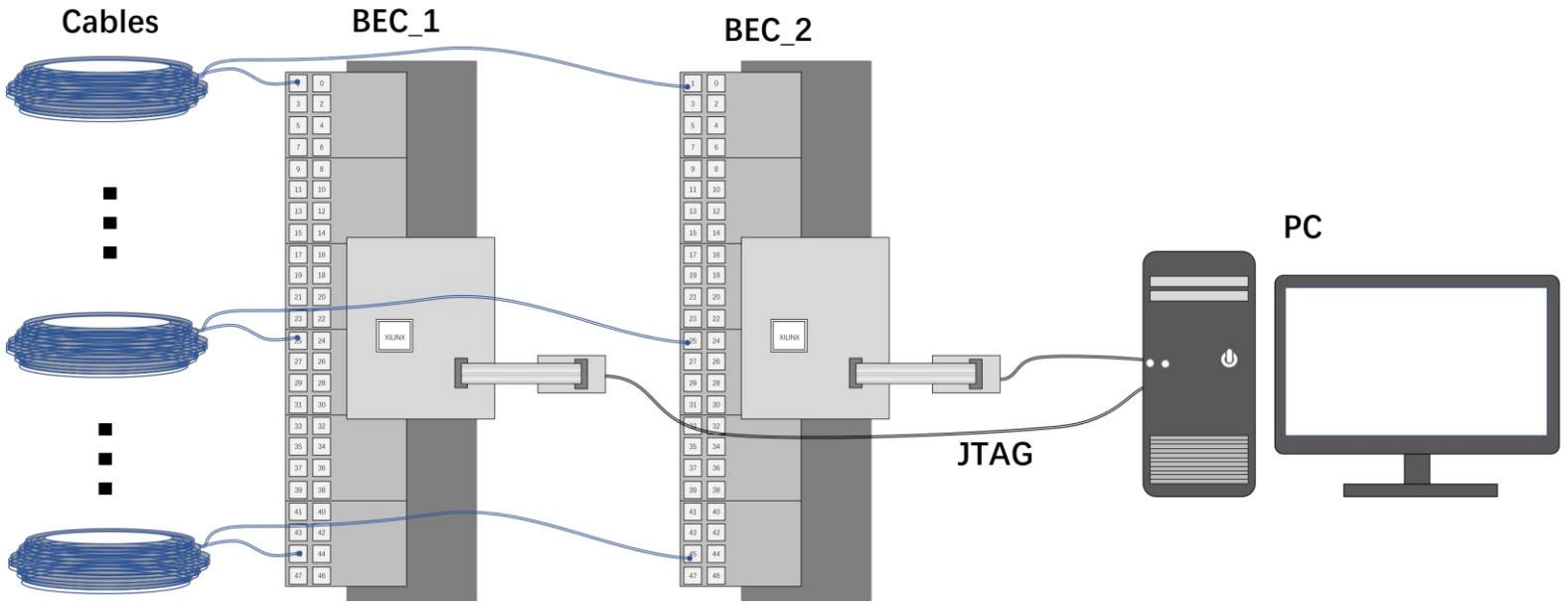
- 23 good channels, 5 bad channels
- BER of good channels ≤ 1.23×10^{-14}
- The error in channel 44 is due to not optimized sampling point
- The other bad channels are caused by bad cable connectors

Two boards test



Multi-channel closed-loop diagram of two boards test

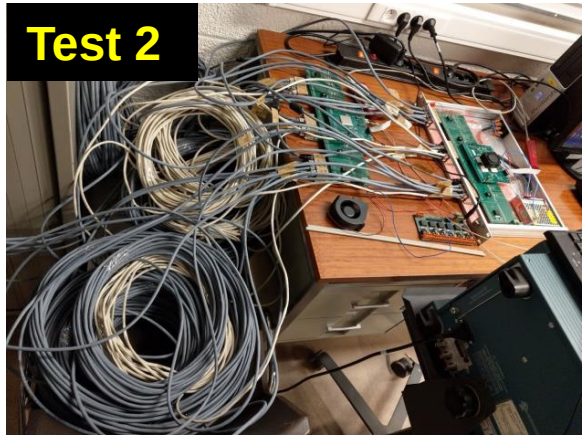
Two boards test ▶ Automatic test plan



Automatic test plan for two boards test

Material needed: Cat5e FTP cables, 1 PC with vivado 2018.1.

Two boards test ▶ Long term test



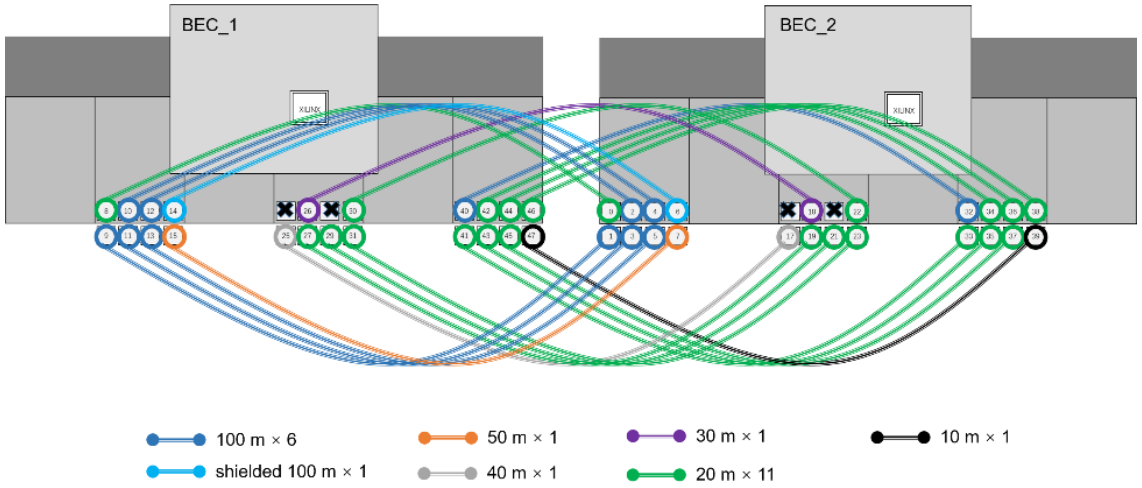
Board1	Board2
1-2(clock)	3-6(counter)
3-6(counter)	1-2(clock)
4-5(prbs)	7-8(checker)
7-8(checker)	4-5(prbs)

- 72 h continuous test
- 22 cables work simultaneously
- 125 Mbps PRBS
- 62.5 MHz clock

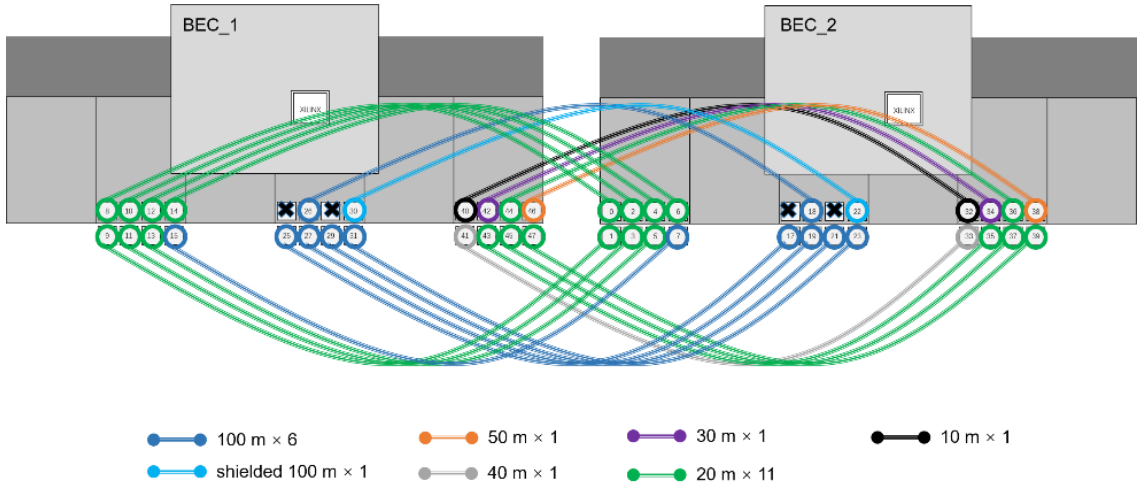
- Special thanks to the IT team (Adriano et al.)

Two boards test ▶ Connection plan

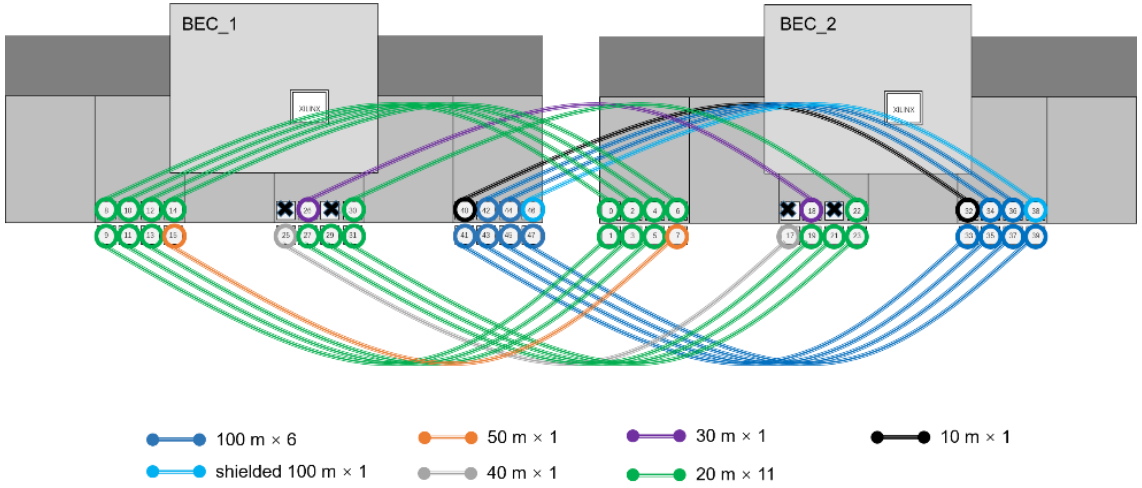
Test 1



Test 3

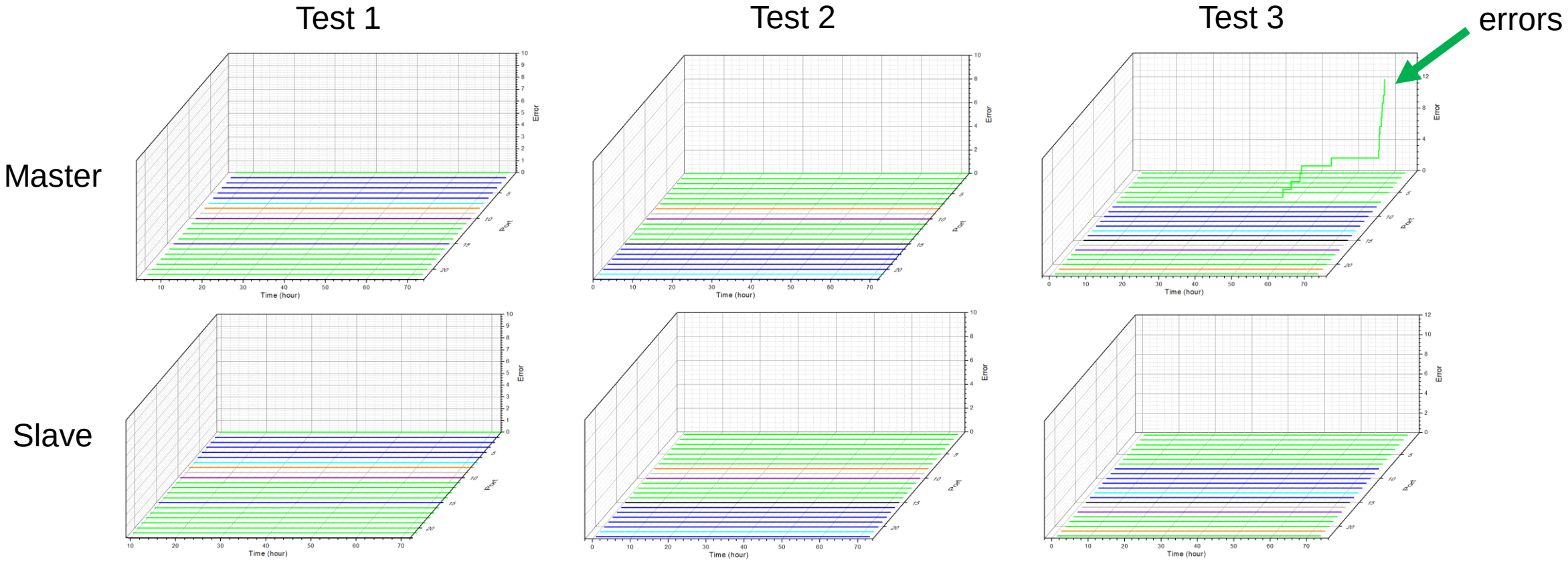


Test 2



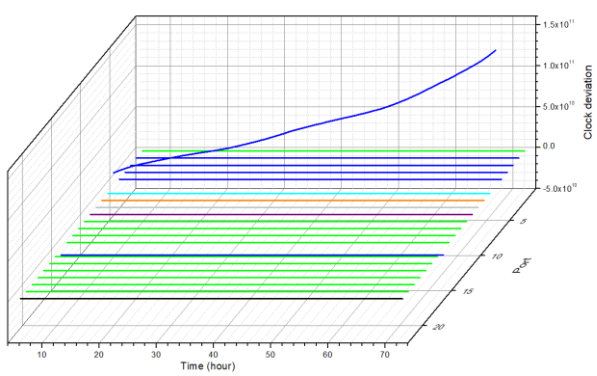
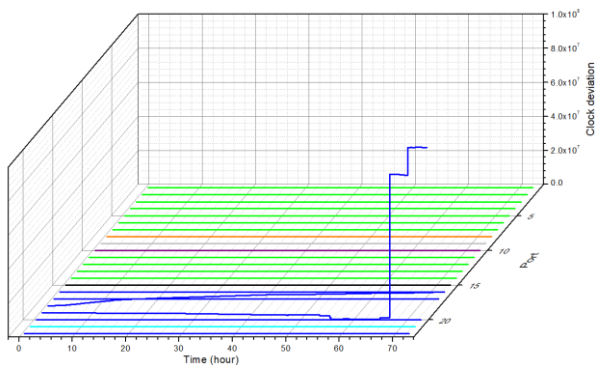
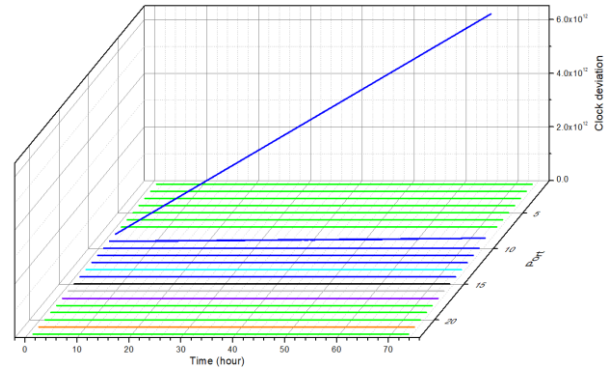
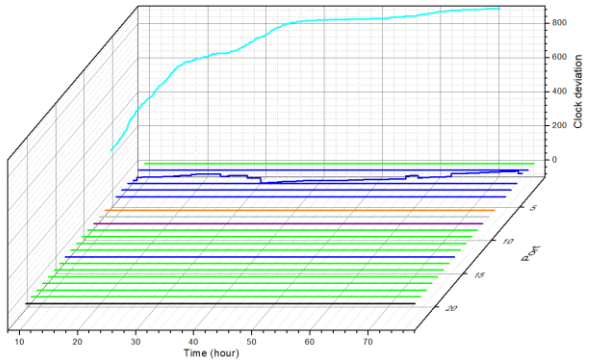
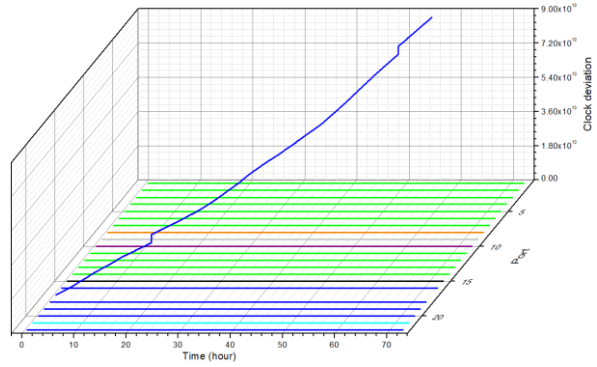
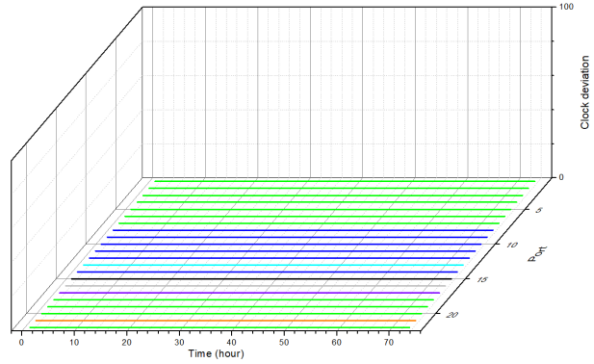
- Port_8 on BEC_1(master) and Port_0 on BEC_2(salve) are connected via a 20 m cable for clock distribution.
- Three 72-hour tests were conducted to enable seven 100 m cables to cover all the slots.

Two boards test ▶ PRBS error check



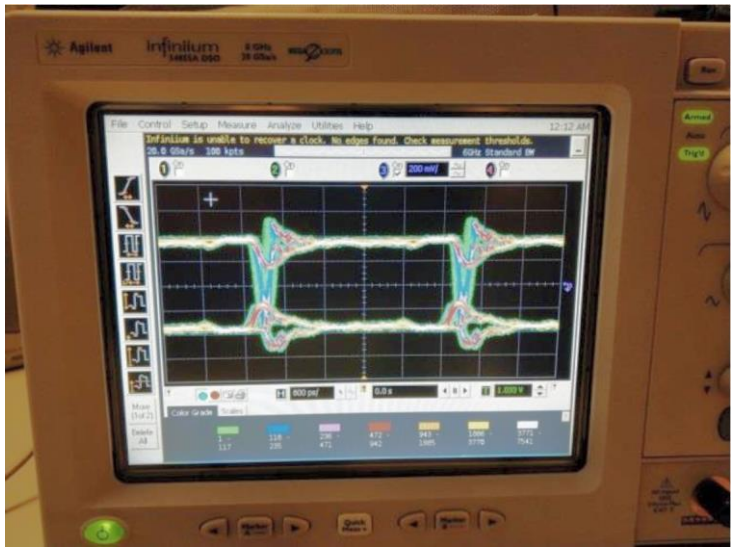
- Only channel 13 in test 3 has 16 errors, the bit error rate is lower than 4.9×10^{-13}
- It's due to not optimized sampling point

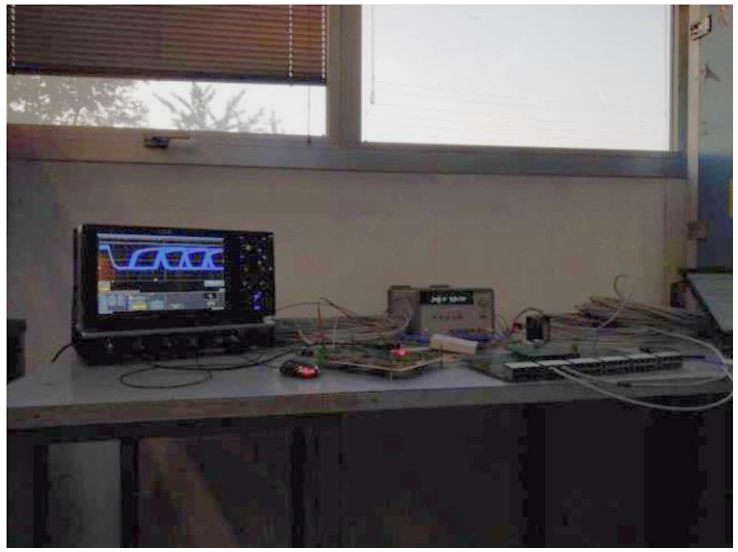
Two boards test ▶ Clock error check

	Test 1	Test 2	Test 3
Master			
Slave			

- A toy emulation of multiple GCU due to lack of real hardware
- This path will be used for IEEE1588 data in real application

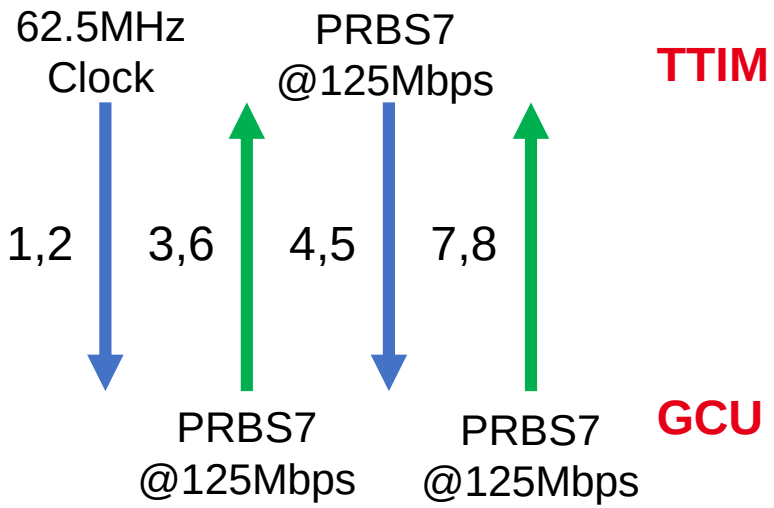
Combined test ▶ Padova





- Only have time to perform short term test.
- No problem found.

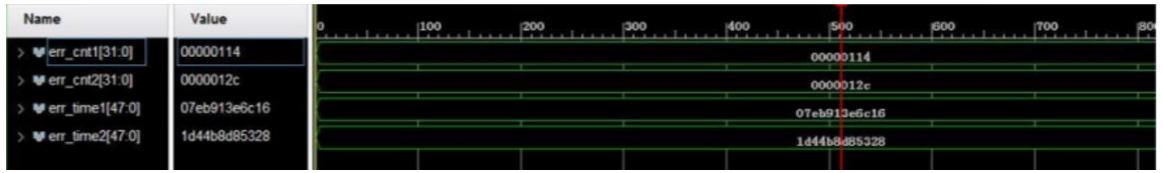
Combined test ▶ Beijing



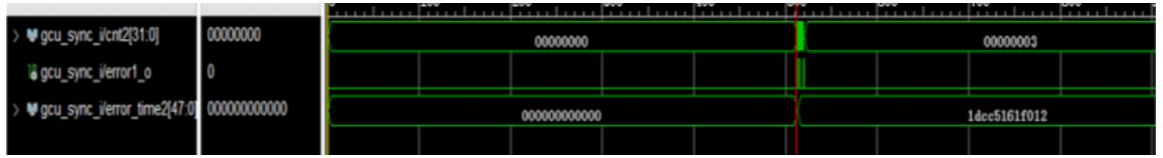
Test firmware structure

Combined test ▶ Beijing

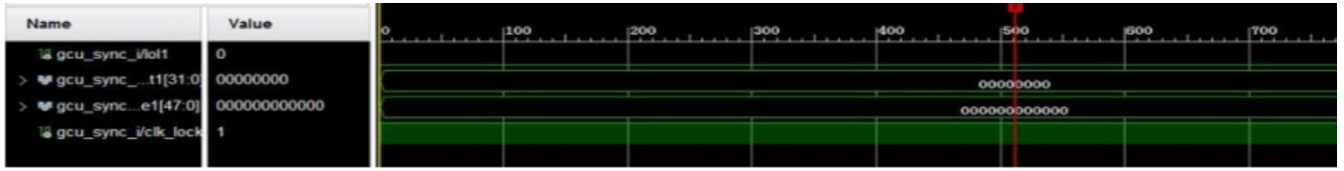
TTIM 3,6 err
TTIM 7,8 err



GCU 4,5 err



GCU 1,2 lock



- No error run for 60 hours

Cable pairs	BERs (60 hours)		BERs (72 hours)	
1,2 (GCU1/2)	No loss of lock	No loss of lock	No loss of lock	No loss of lock
3,6(TTIM)	1.11×10^{-13}	$<3.7\times10^{-14}$	3.4×10^{-12}	4.57×10^{-9}
4,5(GCU1/2)	$<3.7\times10^{-14}$	$<3.7\times10^{-14}$	$<3.7\times10^{-14}$	2.09×10^{-10}
7,8(TTIM)	$<3.7\times10^{-14}$	$<3.7\times10^{-14}$	3.7×10^{-12}	9.91×10^{-11}

- Errors are due to external noise

Conclusion

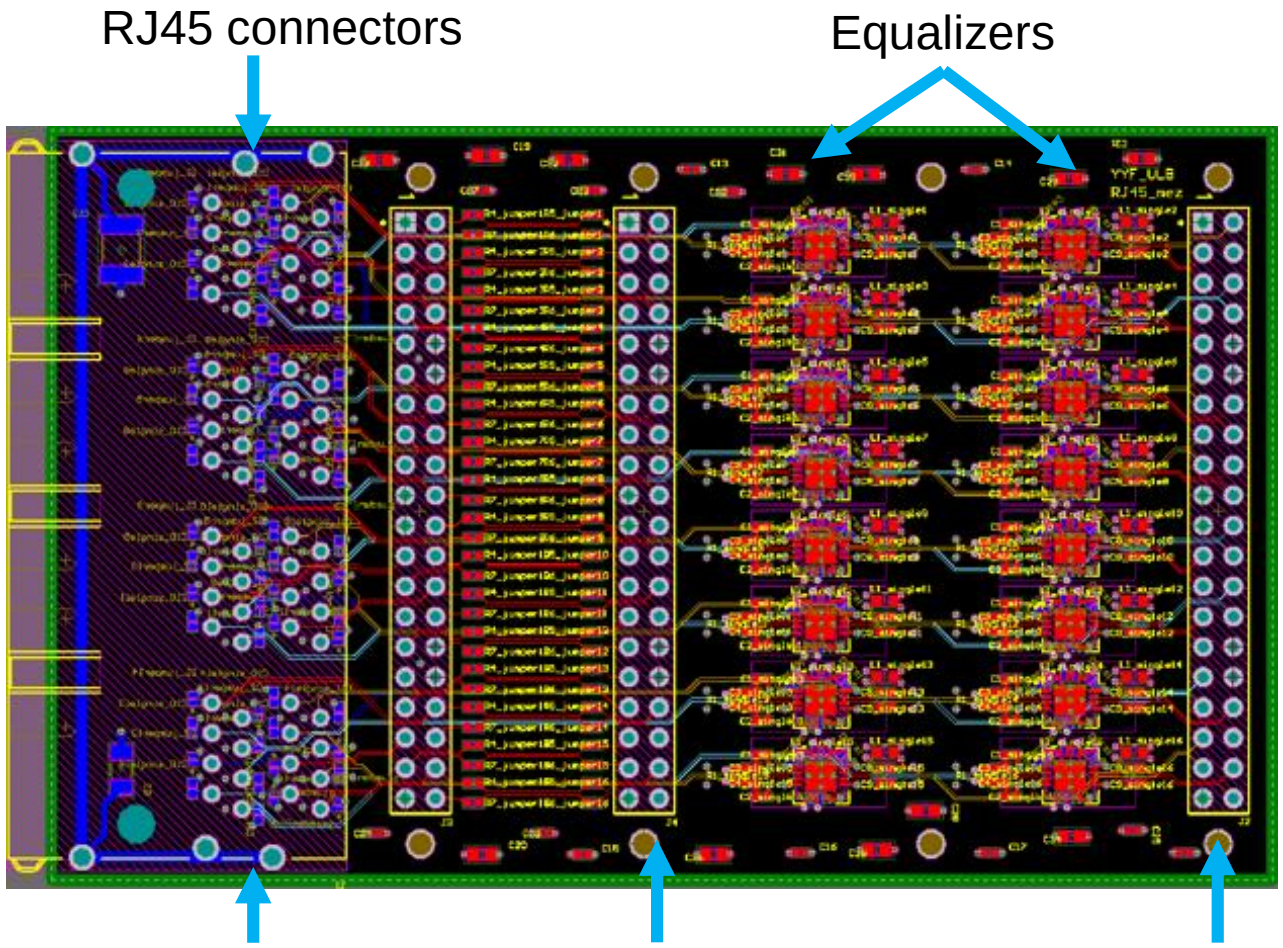
- BEC v4 have been tested in different manners and at different places, no evidence of hardware design failure has been found.
- More realistic combined tests with 48 GCU and real JUNO cable is necessary before mass production, it is foreseen in December in Padova.
- Transmission control protocol is necessary if perfect shielding can not be achieved

Conclusion ▶ Production plan

- Final prototype (5 BEC) in November 2019
- Test from December 2019 to January 2020
- Pre-production (10 BEC) in March 2020
- Mass production (140 BEC) from July to August 2020
- Aging and function test from October to November 2020

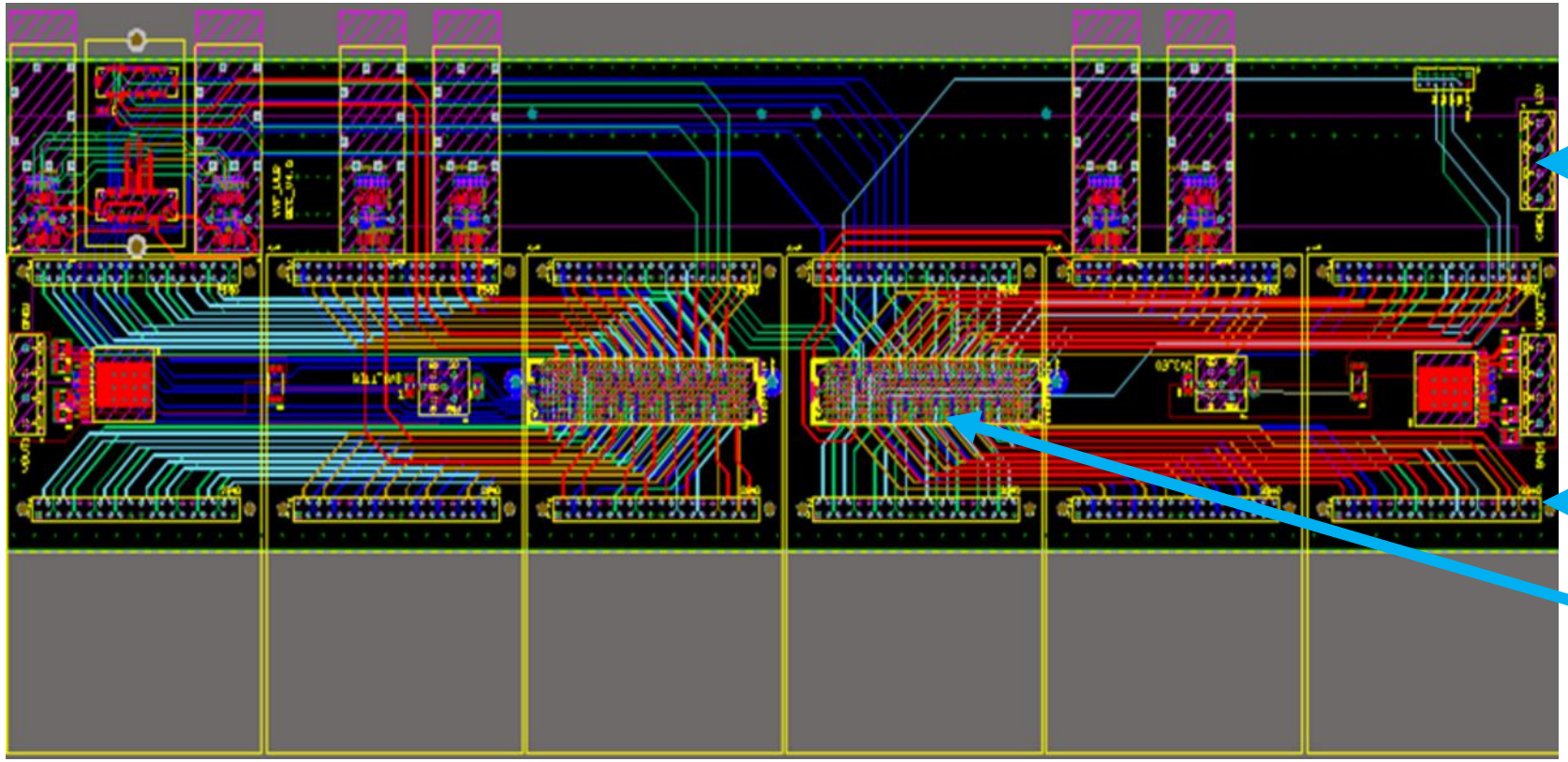
Thanks !

Latest design of BEC ▶ Mezzanine card



- 103 cm × 63 cm
- 8 layers
- 32 differential pairs with impedance control
- All equalizer inputs route in stripline covered by solid GND and VCC
- Use multi-channel design for all the equalizers
- 6 channels have reference layer cutout under ac coupling

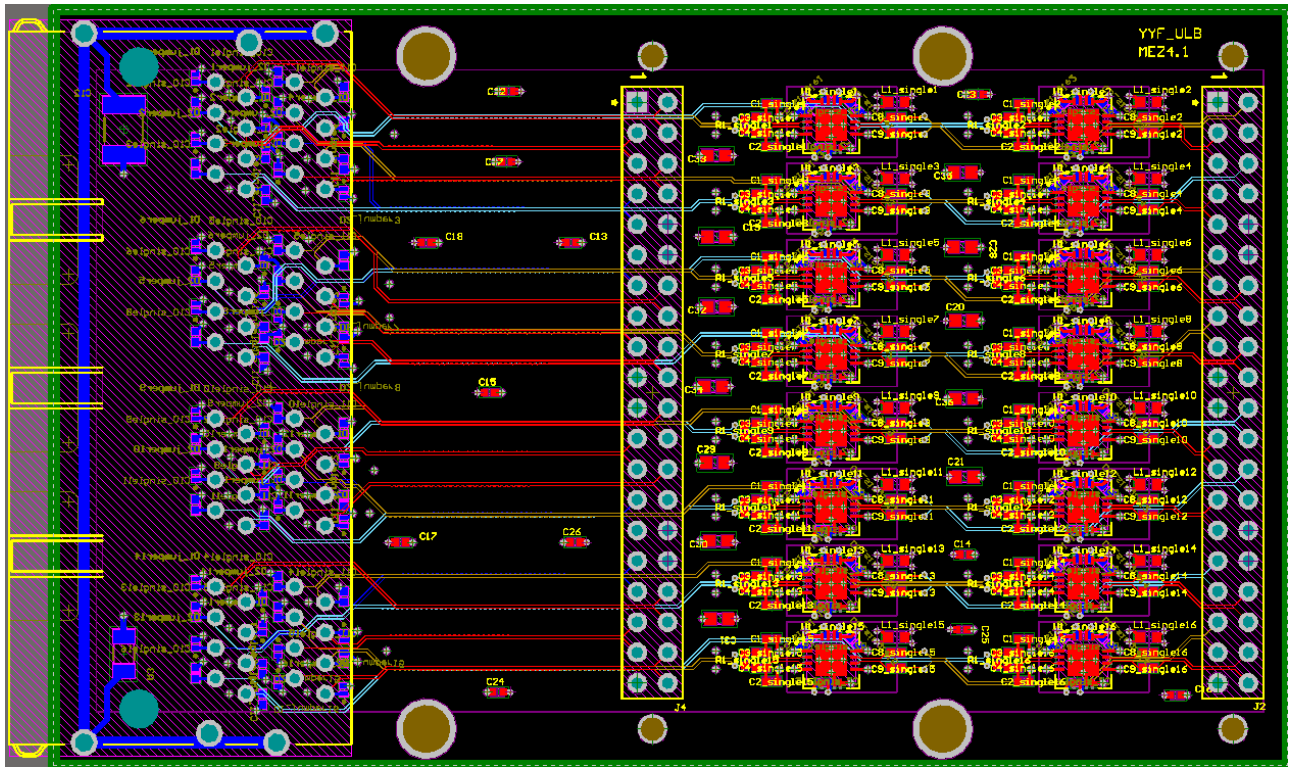
Latest design of BEC ▶ Base board



- 100 cm × 383 cm, 10 layers
- Supply power to TTIM and mezzanine separately, 10 A each
- 196 differential pairs with impedance control

Future work ▶ BEC v4.1

Future optimization for V4.1



- Add TVS protection
- Remove 0 ohm on tx path
- Make equal length for all the rx
- Cover rx with solid GND
- Recover all the cutout of reference