The CMS Cathode Strip Chamber Upgrade for HL-LHC

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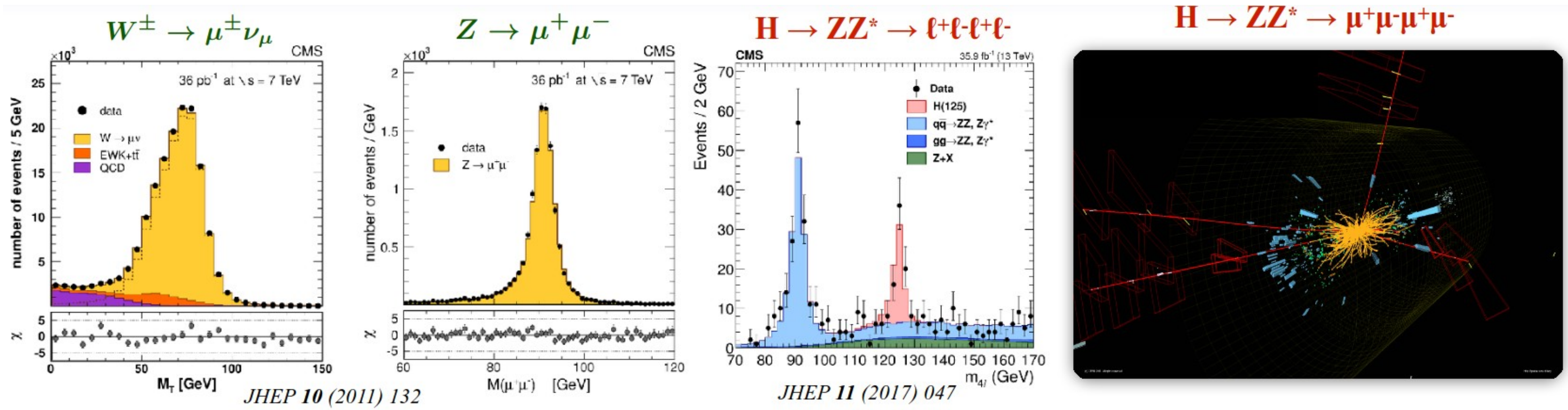
Outline

- ✶ The CMS muon system
- ✶ The CMS Cathode Strip Chambers (CSCs)
  - ✫ CSC technology
  - ✫ upgrade motivation
  - ✫ LS2 upgrade
  - ✫ re-commissioning
  - ✫ performance
  - ✫ LS3 upgrade
- ✶ Bonus: The GEM-CSC trigger

Muons are key signatures

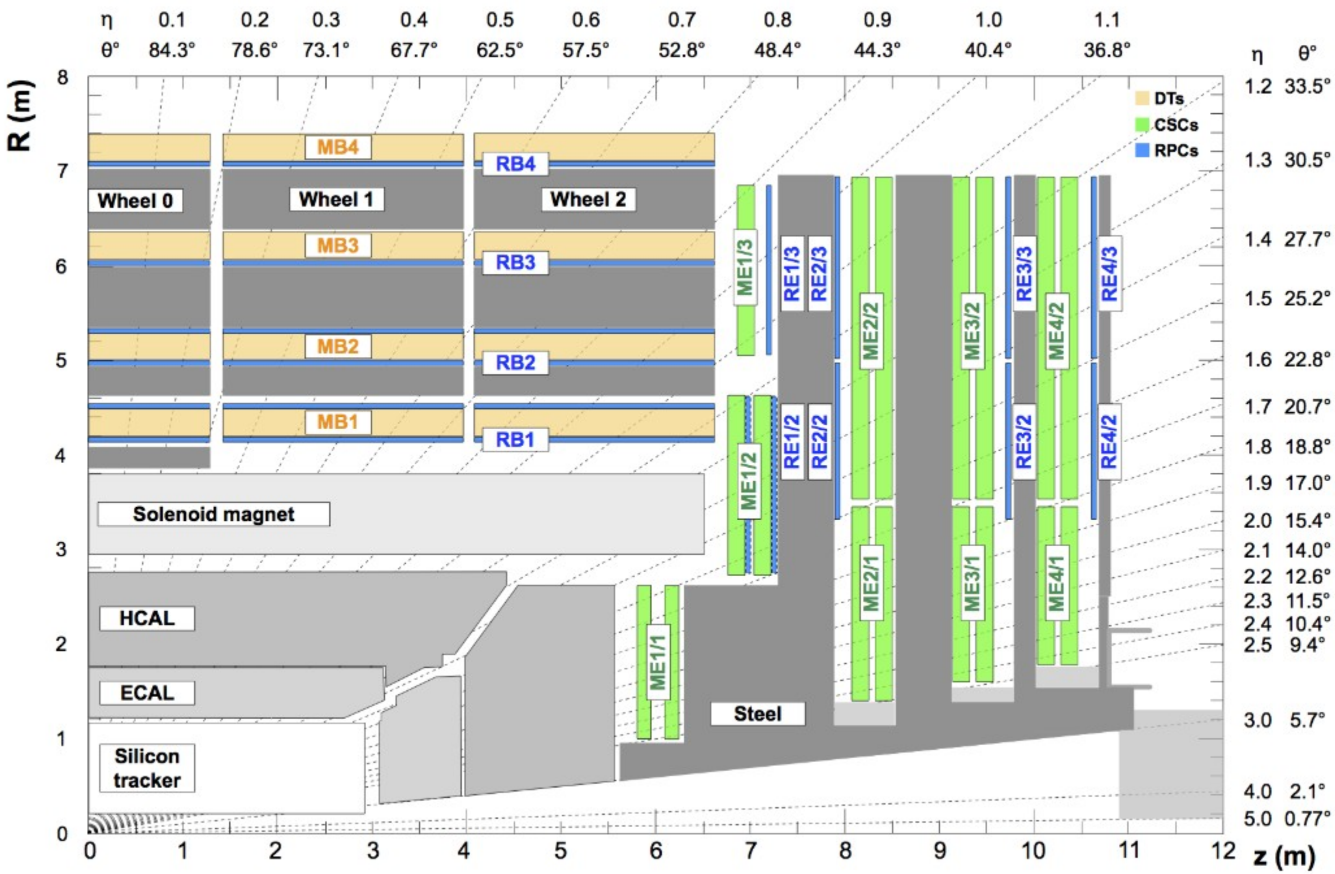


Muons are key to

- reconstruct Standard Model particles such as W, Z, or Higgs
- searches for new physics

One of the main design goals of CMS was to have a **very good** and **redundant muon system**

CMS muon system



DT (drift tubes):
trigger, precision, low rate

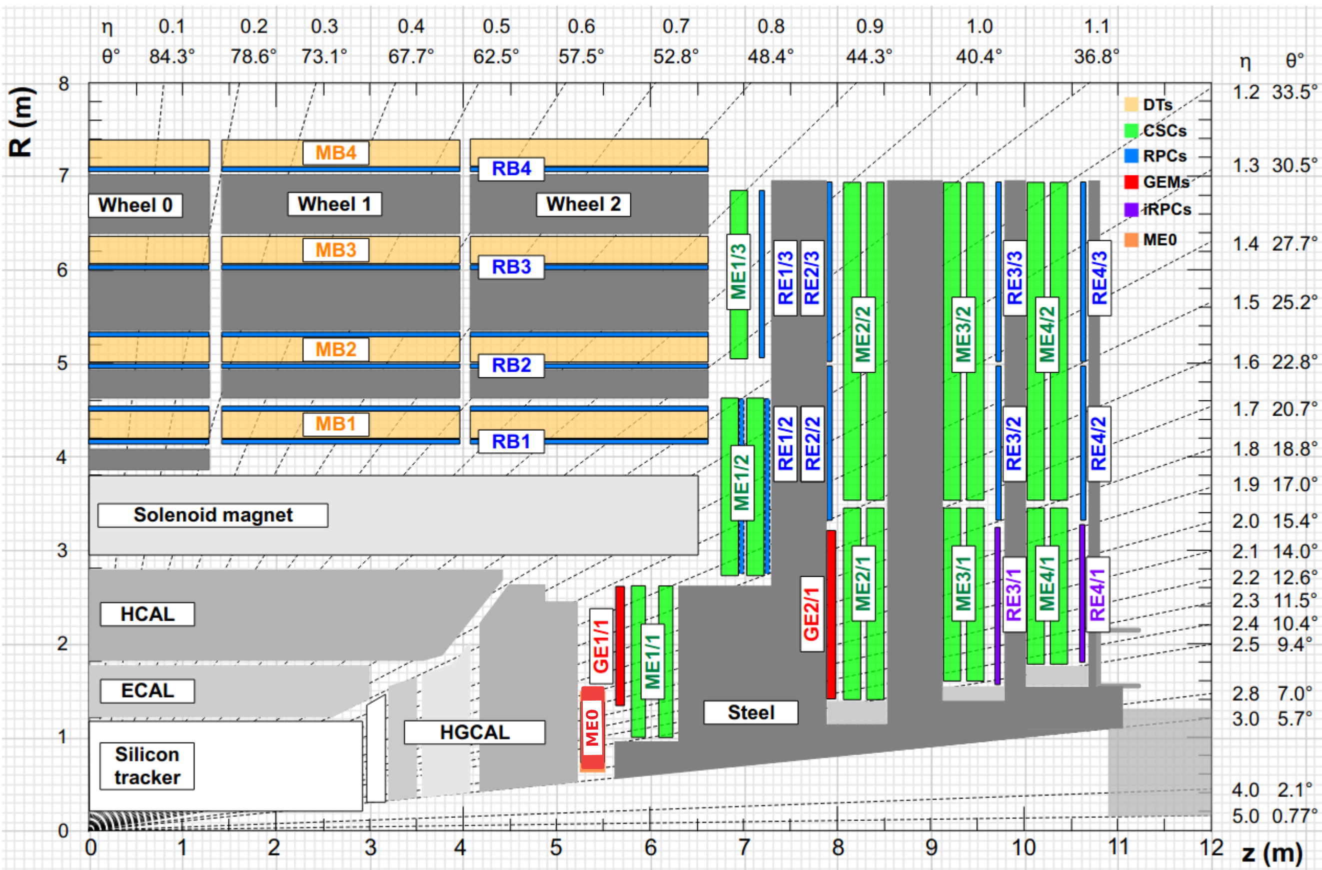
CSC (cathode strip chambers):
trigger, precision, high rate

RPC (resistive plate chambers):
trigger, fast

Redundancy (2 detector technologies on the path of a muon in nearly all directions) ensures

- ✶ robust trigger
- ✶ efficient reconstruction

CMS muon system for HL-LHC



DT, CSC, RPC detectors remain

→ upgrade electronics to cope with HL-LHC rates and enhance performance

New detectors to strengthen tracking in the challenging forward region:

GEM detectors

- ME0: 6 layers, extend coverage to $2.4 < |\eta| < 2.8$
- GE1/1: 2 layers
- GE2/1: 2 layers

Improved RPCs:

- RE3/1: 1 layer
- RE4/1: 1 layer

CSC technology

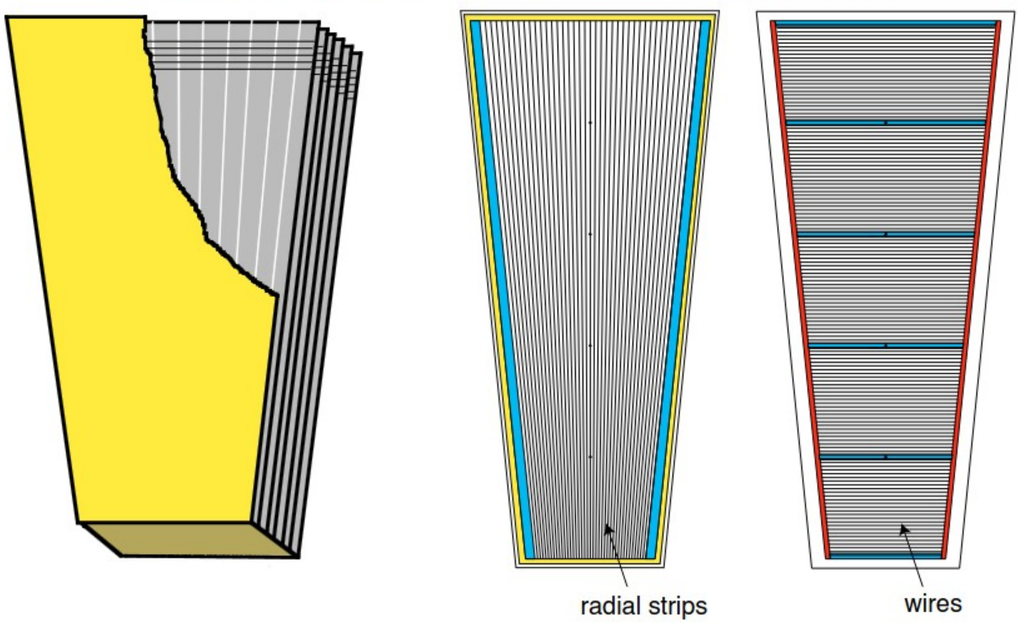
CSC chamber

6 independent layers that measure points (hits) along the trajectory of muons

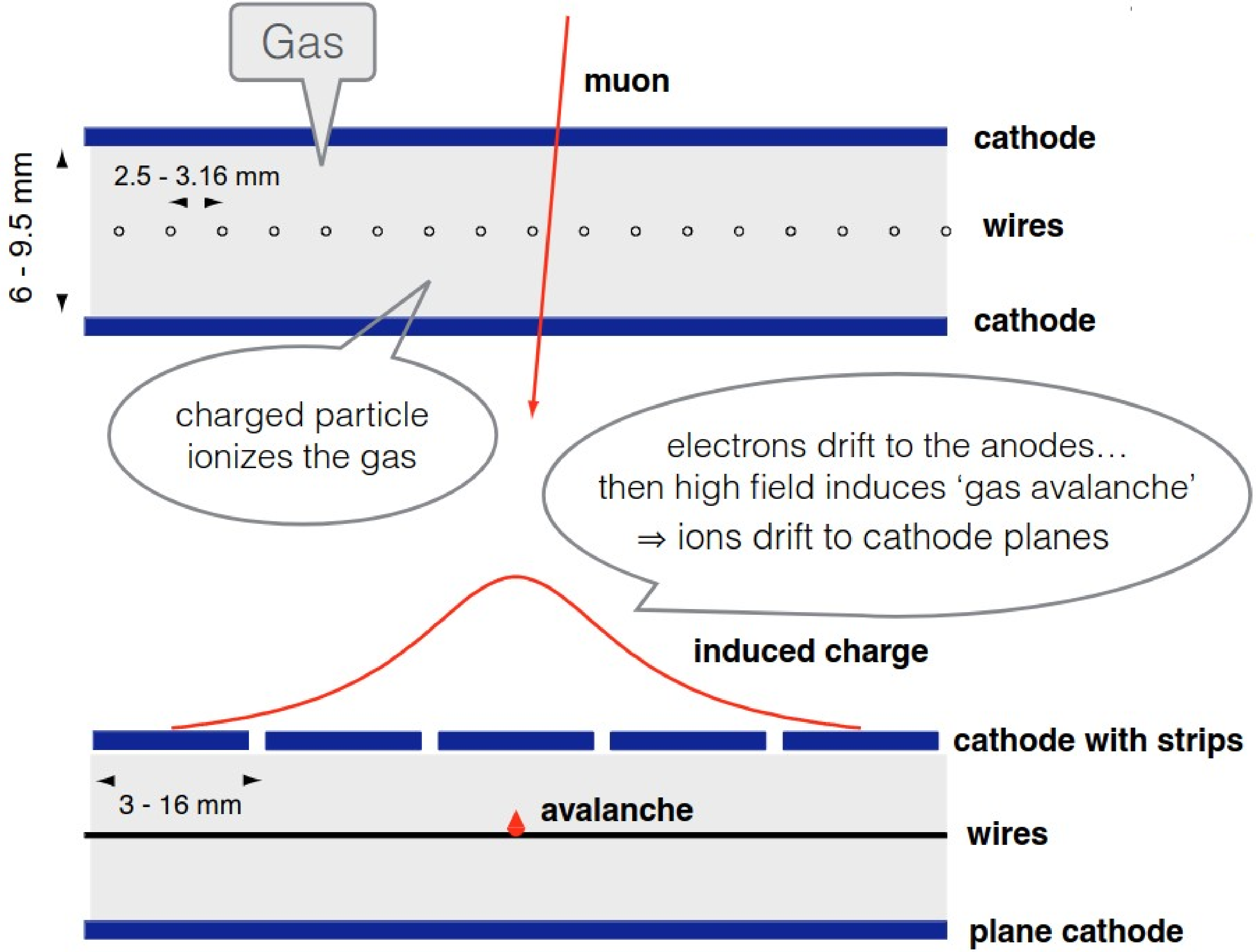
- ✶ 7 cathode panels forming 6 gas gaps
- ✶ 6 of the cathode panels are segmented into radial strips (measure φ)
- ✶ 6 wire layers (anode) in the middle of each gas gap running transversally

Open ME2/1 CSC being inspected at PNPI

6 strip-wire layers running orthogonally in each CSC



CSC chamber

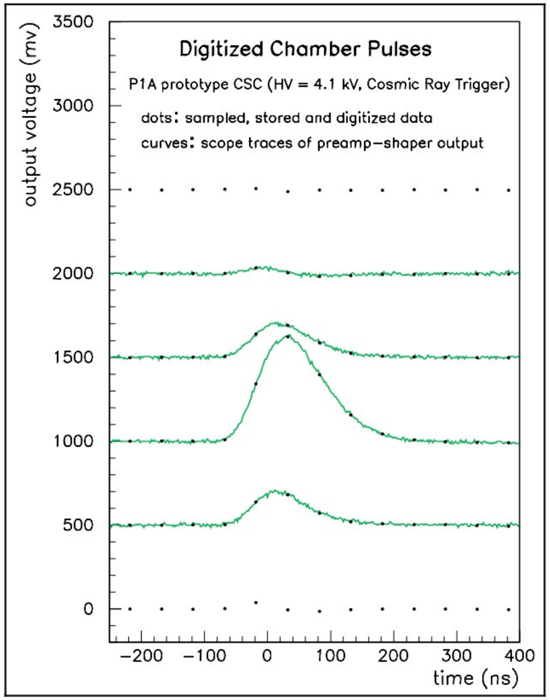


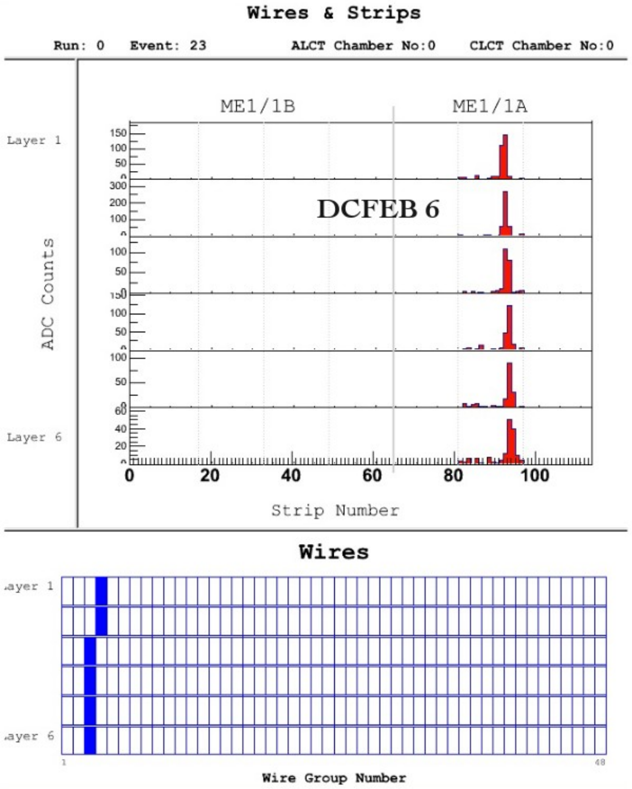
electrons drift to anode inducing an electron avalanche
→ inducing signal on wires

ions drift to cathode
→ inducing a charge on the strips

CSC chamber

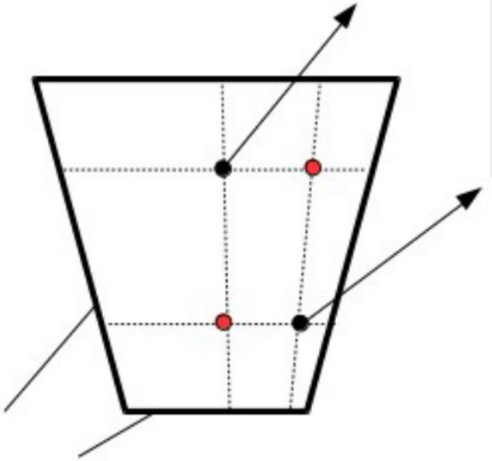
- ✶ center-of-mass fit of cathode signal provides precision measurement φ → pT
- ✶ fit to 8 cathode time samples provides precision time measurement



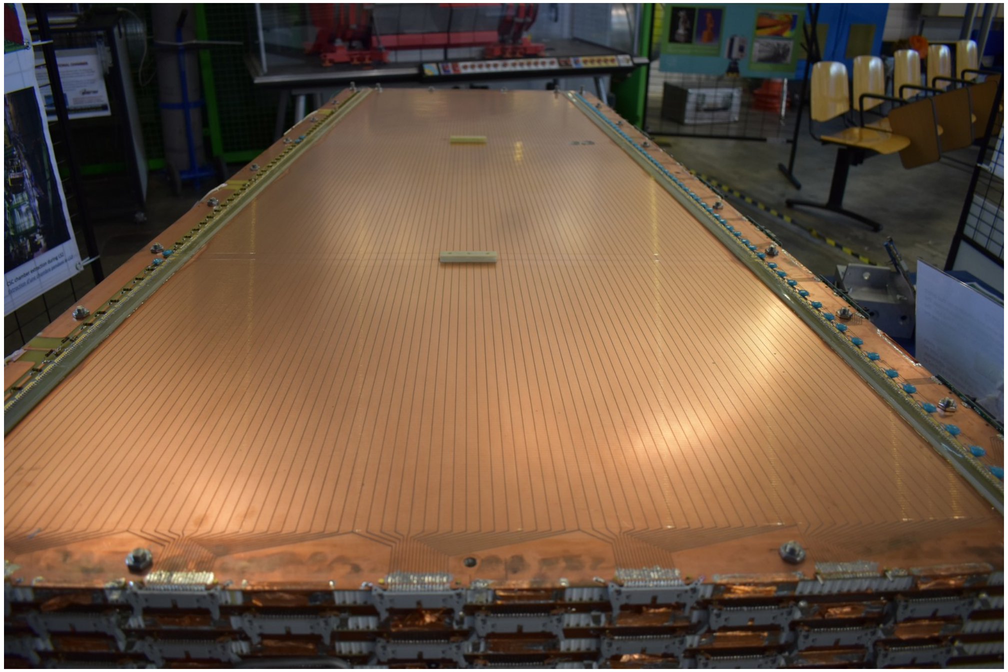


coincidences of anode and cathode signals form hits

note: more than 1 muon per chamber leads to **ghosts**



Advantages of CSCs



- Intrinsic spatial resolution, basically defined by signal-to-noise ratio, can be as good as 50 μm
- Closely spaced wires make the CSC a fast detector
- By measuring signals from strips and wires, one easily obtains 2 coordinates from a single detector plane
- Strips can be fan-shaped to measure the φ-coordinate in a natural way
- CSCs can operate in large and non-uniform magnetic field without significant deterioration in performance
- Gas mixture composition, temperature, and pressure do not directly affect CSC precision and thus stringent control of these variables is not required
- Detector mechanical precision is defined by strips which can be etched or milled with the required accuracy and can be easily extended outside the gas volume, thus making survey of plane-to-plane alignment very simple

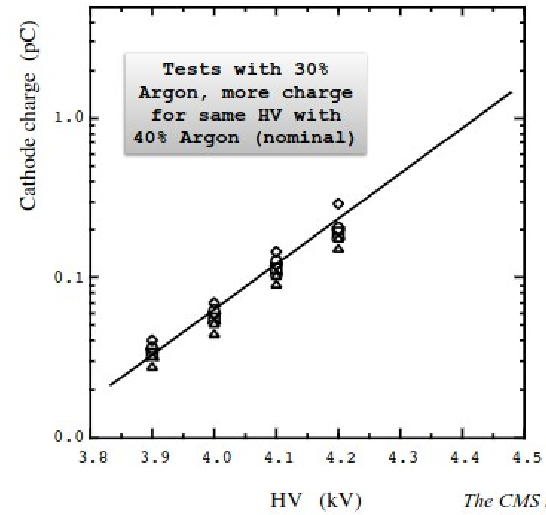
Gas and High Voltage

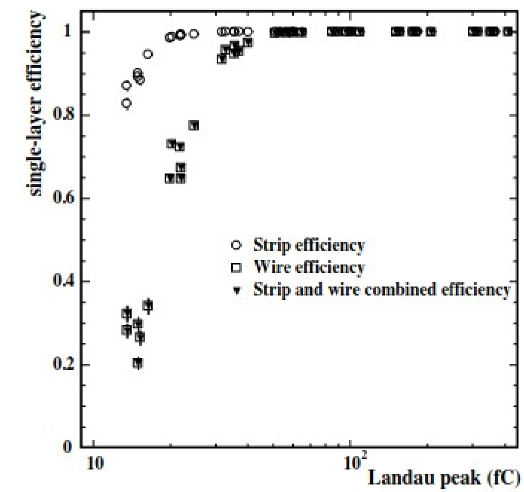
CSCs use a gas mixture of
CO_2 (50%) + Ar (40%) + CF_4 (10%)

- **Ar** produces the ionization
  → more Ar lowers the operating voltage
- **CO_2** is non-flammable quenching gas
  → helps stabilize operation by minimizing spurious pulses through absorption of photons
- **CF_4** also quenches, but is added because it prevents aging in wire chambers
  - expensive, corrosive greenhouse gas
    → studying how to minimize its use or using a substitute

High Voltage system provides **2.9 kV** (ME1/1) and **3.6kV** (non-ME1/1) to the wires

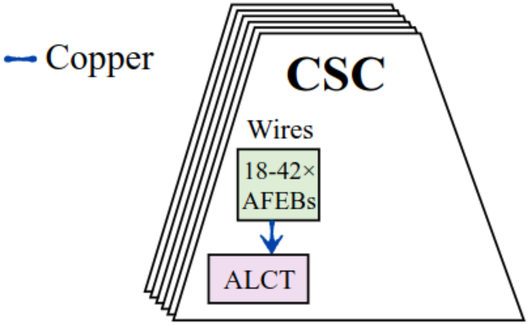
- amount of ionization charge depends on this bias voltage
- need enough charge to ensure optimal efficiency
- **working point** on efficiency plateau but **close to knee** in order to **minimize** charge and thus **aging** of the chambers





The CMS muon project: TDR, CERN, 1997

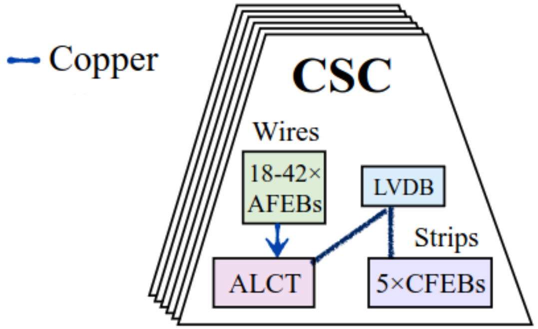
Electronics



AFEB (Anode Front-End Board): amplifies signals from the anode wires and sends hits to the ALCT. There are 18-42 AFEBs per CSC

ALCT (Anode Local Charged Track board): finds patterns among the six-layer anode hits sent by the AFEBs consistent with muon stubs, and sends the two with the most layer hits to the TMB

Electronics



L1A: Level 1 Accept, signal from CMS trigger that we want to keep this event

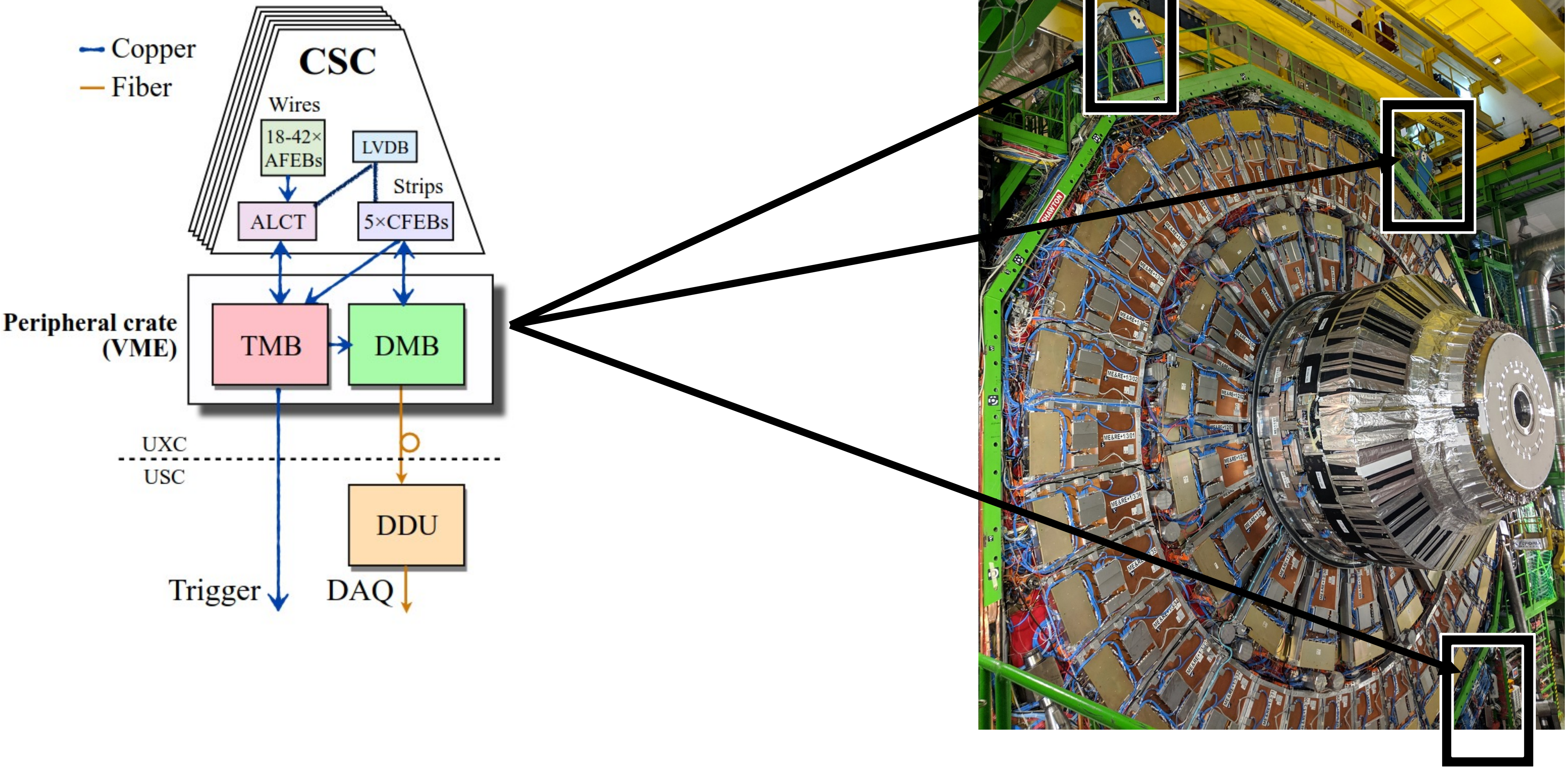
AFEB (Anode Front-End Board): amplifies signals from the anode wires and sends hits to the ALCT. There are 18-42 AFEBs per CSC

ALCT (Anode Local Charged Track board): finds patterns among the six-layer anode hits sent by the AFEBs consistent with muon stubs, and sends the two with the most layer hits to the TMB

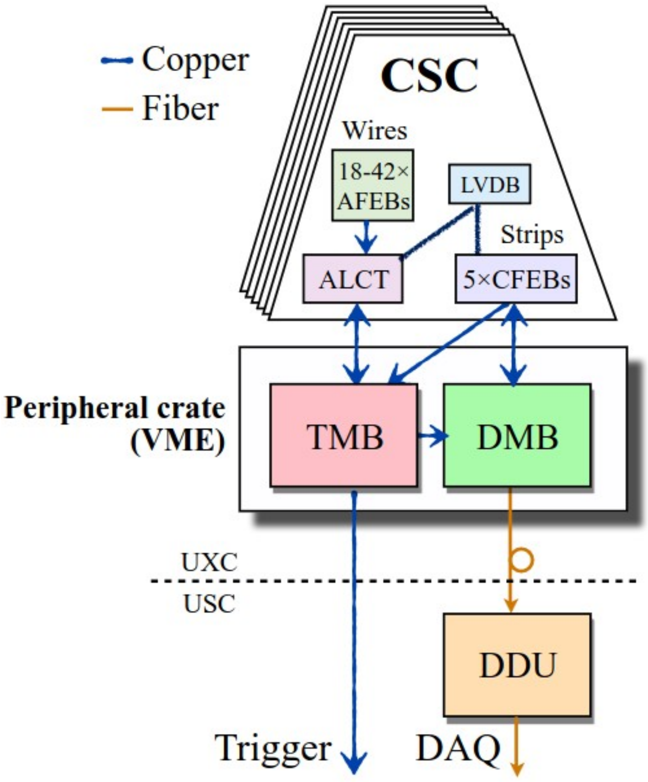
CFEB (Cathode Front-End Board): amplifies signals from the cathode strips, sends fast trigger information to the TMB, and, upon receiving an L1A, digitizes the strip signal waveforms and sends them to the DMB. There are typically 5 CFEBs per CSC

LVDB (Low Voltage Distribution Board): distributes the low voltage power at the appropriate voltage levels to the on-chamber boards

Electronics



Electronics



TMB (Trigger MotherBoard): sends coincidences between cathode hit patterns and anode hit patterns (local charged tracks or LCTs) to the MPC (trigger path) and, upon receiving an L1A, to the DMB as well

DMB (Data acquisition MotherBoard): upon arrival of an L1A, it collects anode, cathode, and trigger information and sends it to the DDU. It also controls the CFEBs on a chamber

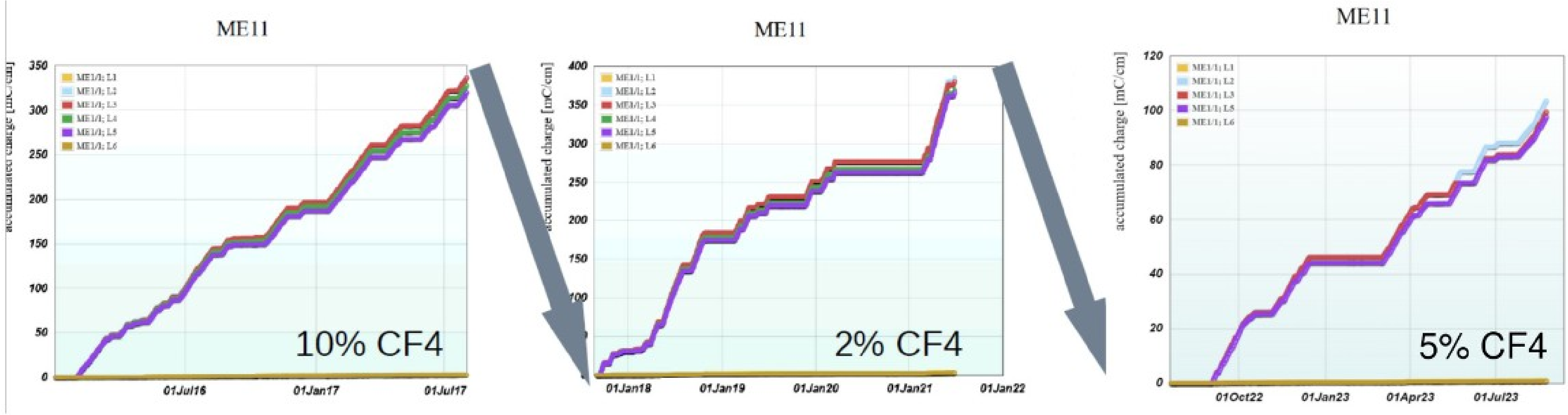
DDU (Detector-Dependent Unit): upon arrival of L1A, collects data from all 15 DMBs in a CSC sector, sends the information to the global DAQ path

= FED

Longevity studies

Studies at GIF++ irradiation facility:

- irradiation using strong Cs source
- performance study using muon beam (up to 100 GeV) in combination with photon field from Cs source



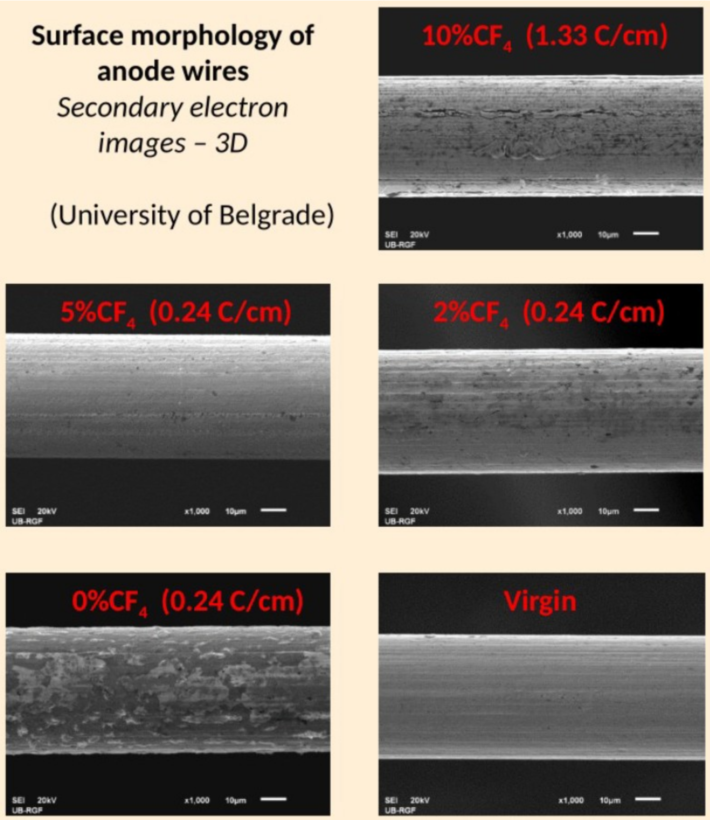
Q [mC/cm]	Expected* Q(HL-LHC)	10%CF4	+ 2%CF4	+ 5%CF4**	Total
ME1/1	200	330	370	100	800
ME2/1	130	330	-	300	630

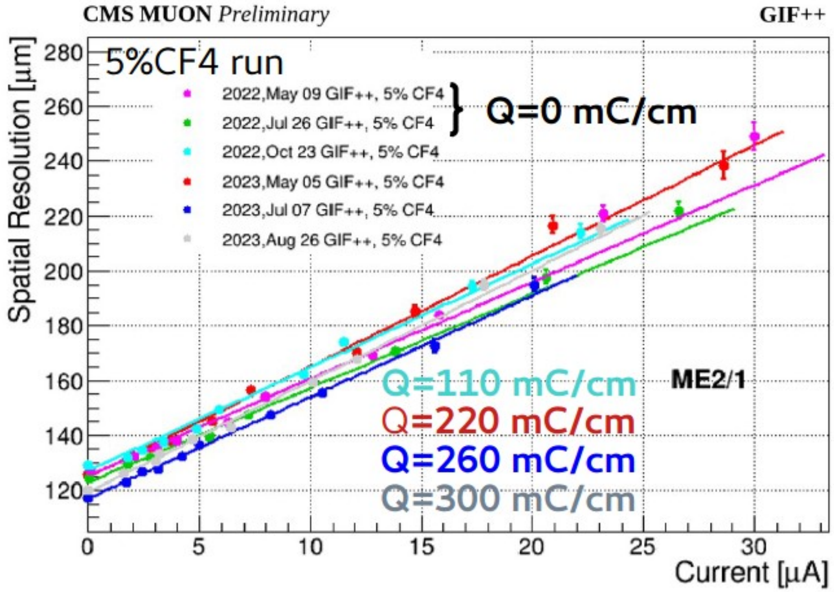
→ no performance degradation observed with nominal gas mixture (10% CF_4)

Reduction of CF_4

Lab studies with 5%, 2%, 0% of CF_4:

- ✶ no performance degradation observed
- ✶ but anode wire deposition was observed for 0 and 2% CF4 up to 300 mC/cm





Longevity study ongoing at GIF++ for promising mixture
Ar (40%) + CO_2 (55%) + CF_4 (5%)

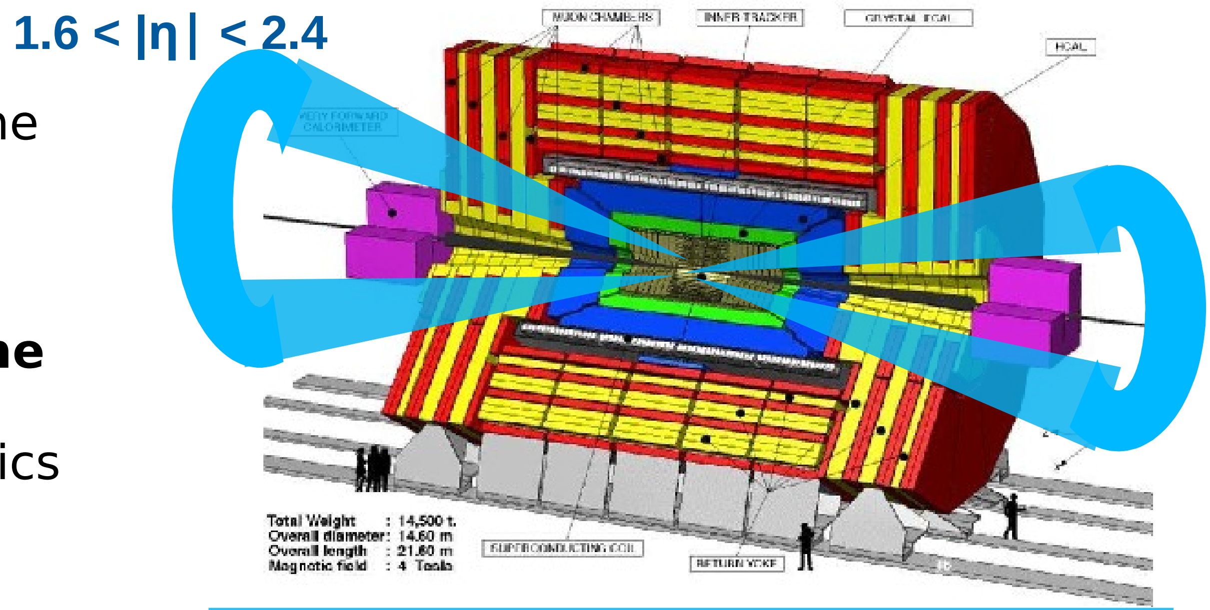
Upgrade motivation

Upgrade motivation

Electronics upgrade of the high-eta CSCs (innermost rings)

Limiting factors of the present electronics:

- **L1 trigger rate:** old CFEBs do not have enough buffering for chambers closest to beamline
- **Longer L1 trigger latency:** required for new track trigger
- Output **bandwidth** and **pipeline length** (not enough BRAM in Virtex-E FPGA) of ALCT electronics not sufficient
- GBTx (instead of EEPROM) programming to mitigate EEPROM failures experienced in 2017 in high-occupancy CSCs (ME1/1)

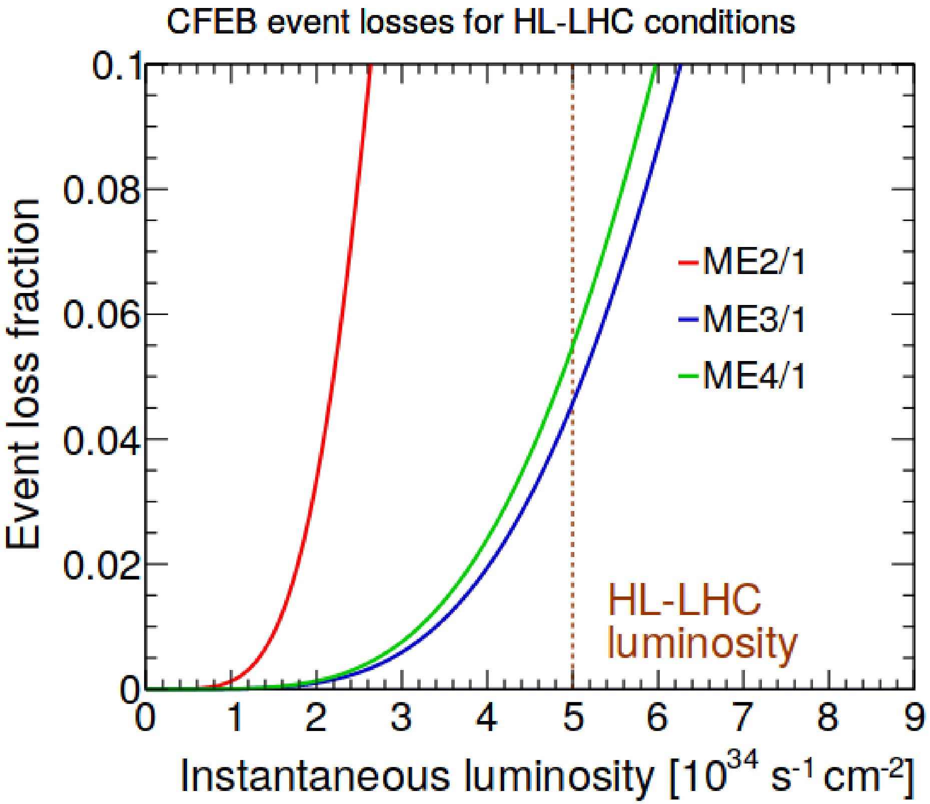


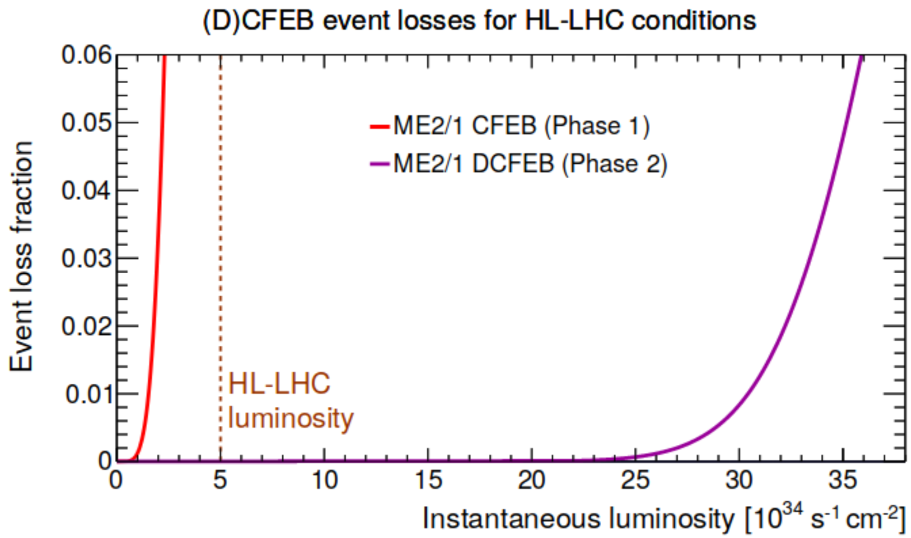
Approximate angular region of the inner rings:
ME1/1, ME2/1, ME3/1, ME4/1
= 180/540 chambers

Upgrade motivation

Expected data loss with legacy electronics due to:

- insufficient buffer size of front end electronics
- longer latency requirements
- insufficient output bandwidth due to higher L1 trigger rates and occupancy



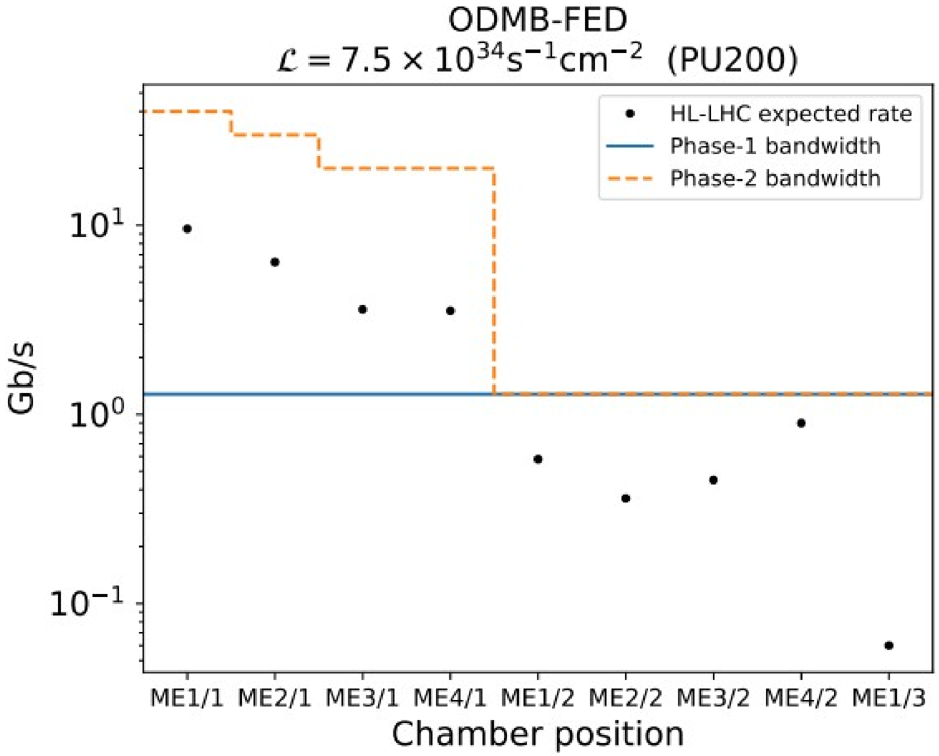


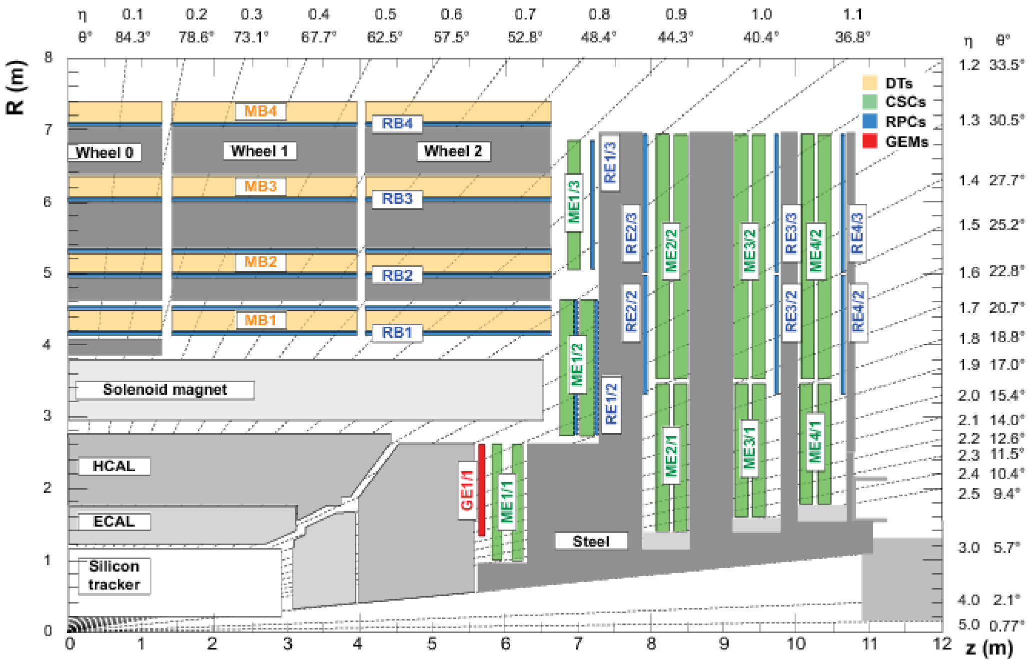
Expected to lose entire ME2/1 ring with old CFEB
→ no data loss with upgraded DCFEB

Upgrade motivation

Bandwidth of ODMB output (currently 1 Gb/s) insufficient for expected HL-LHC rates

→ upgrade of ODMB, optical links, and redesign of backend with ATCA technology





Radiation hardness

Electronics need to survive high rate of collision and background particles, especially in inner ring chambers

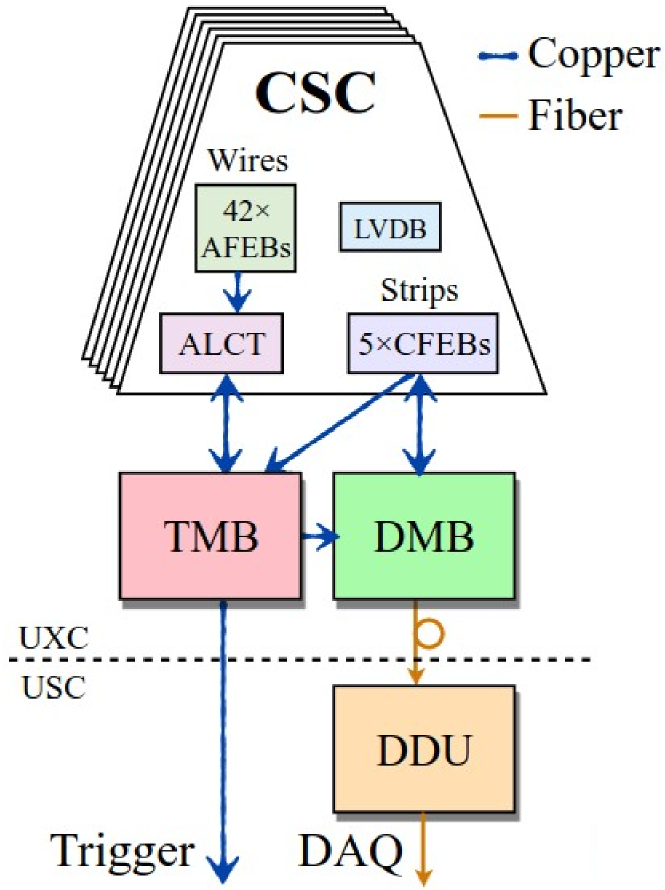
→ new boards and components (optical transceivers, regulators, EPROM, ...) underwent radiation tests

at CHARM, CERN (mixed hadron spectrum)
Texas A&M cyclotron (neutrons)
UC Davis cyclotron (protons)

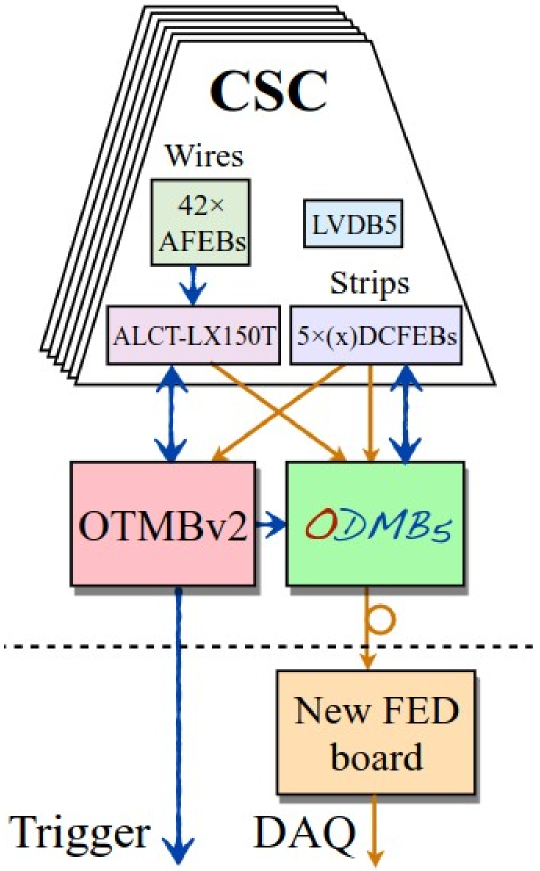
- total integrated dose up to 300 Gy
(3x expected 100 Gy for 3000/fb at HL-LHC)

- susceptibility of electronics to single-event upsets (SEUs)
change of state caused by one single ionizing particle striking a sensitive node in a micro-electronic device
  - study SEU rate and electronics deadtime

Upgrade Scope

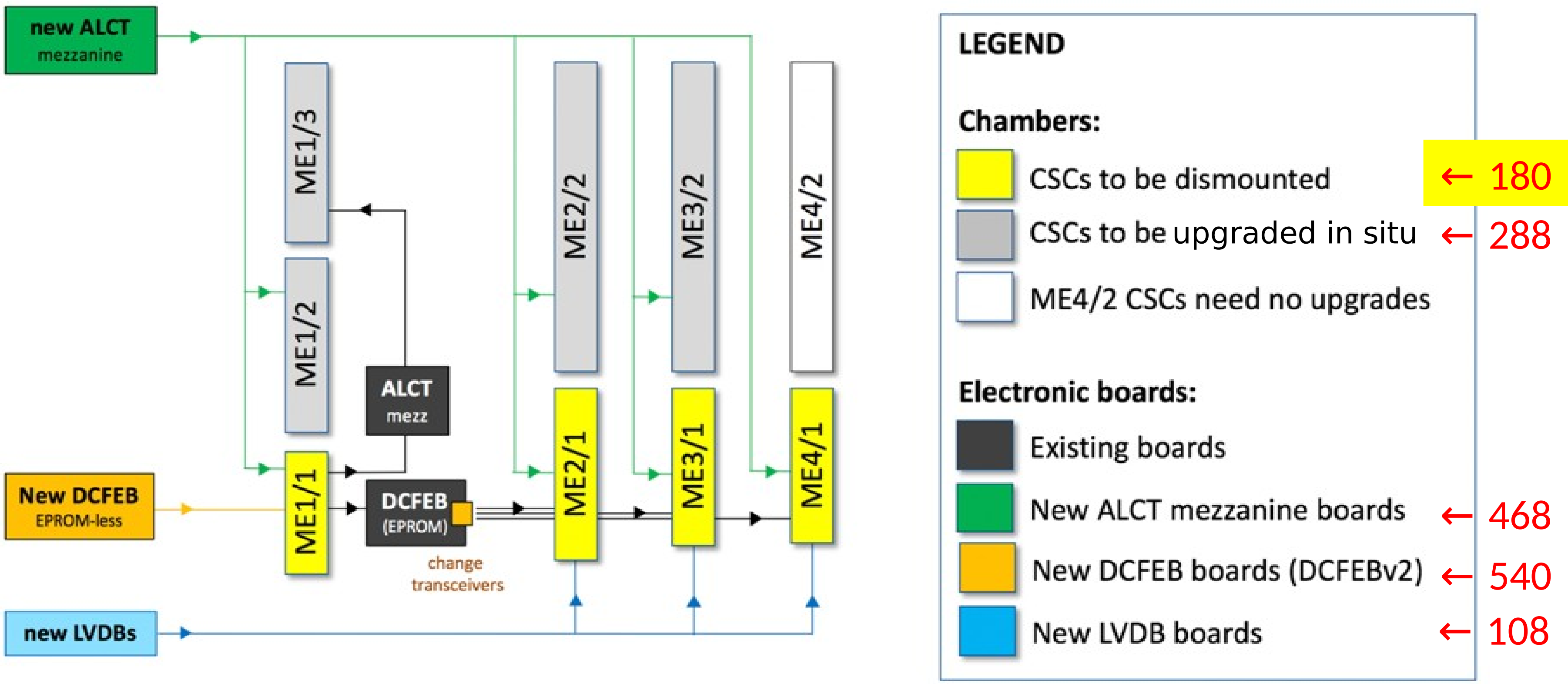


upgrade of the front-end and back-end electronics



LS2 Upgrade (2019 -2020)

CSC LS2 upgrade effort



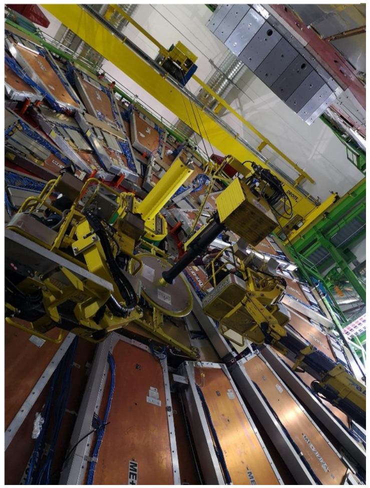
+ OTMBs (peripheral crates) ← 108
+ ME1/1 HV system: custom system with higher current monitoring resolution, as used on other rings to have homogeneous system
+ LV system: to provide appropriate voltages and currents to the new electronics
+ ME1/1 cooling circuit replacement

Electronics Upgrade

Workflow:

- ✶ extract chambers and transport them to lab
- ✶ remove and replace electronics (DCFEBs, ALCT mezzanine, LVDB) and install optical fibers
- ✶ thorough tests of all electronics and chamber components, including data-taking with cosmic rays
- ✶ long-term burn-in to look for early electronics death
- ✶ re-test electronics

lab on the surface

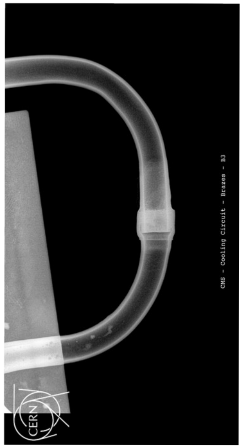


chamber extraction

electronics replacement

ME1/1 cooling circuit

- not part of the electronics upgrade -

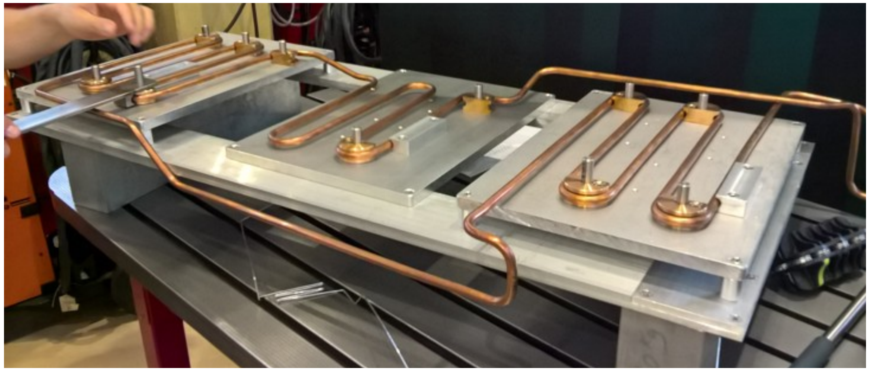


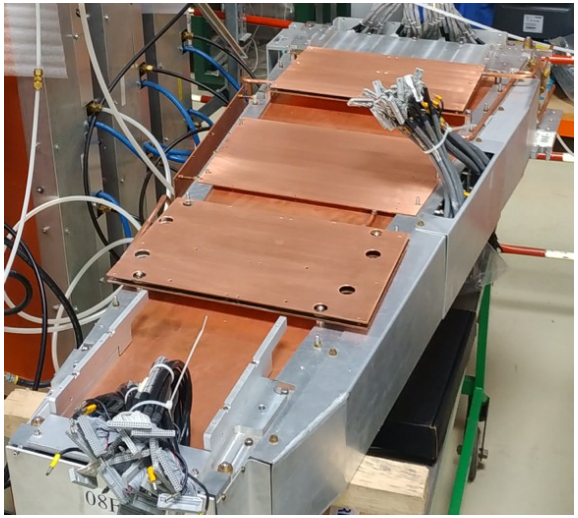
For the ME1/1 chambers there is little space to host all electronic boards. They are attached to cooling plates, both above and under the cooling circuit.

The replacement of electronics puts a lot of strain on cooling circuit (especially to access the bottom boards)

One ME-1/1 cooling circuit was found to be leaky during the refurbishment, and was replaced

- after investigation of the (previously reinforced) joints in the cooling circuit, new cooling circuits were manufactured and installed on all ME1/1 chambers
- the new circuits are constructed from a single pipe, **joint-less** from inlet to outlet





Re-commissioning (2019-2021)

Re-commissioning

Workflow:

- ✶ install and cable chambers
- ✶ quick check of electronic board status and communications without cooling
- ✶ connect cooling & gas → leak test
- ✶ timing scans to find correct parameters for new electronics
- ✶ cosmic data-taking: CSC-only and CMS-wide
- ✶ with beam: trigger primitive timing

Re-commissioning

Trigger Primitive (= anode) timing:

First iteration using single bunch collision runs and CSC results

→ could be biased since no track is required

Then second adjustment using Endcap Muon TrackFinder data (which requires a track)

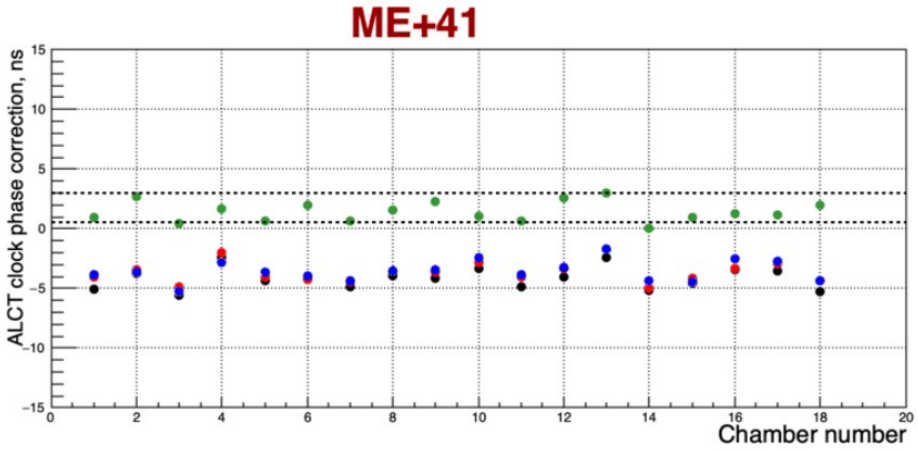
→ systematic shift towards pre-triggering was corrected

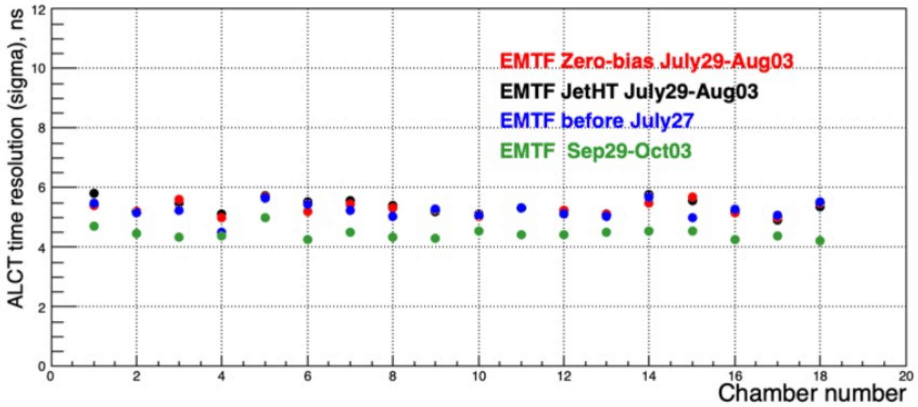
Timing at end of 2022 was relatively good:

- pre-firing probability = $3x10^{-3}$
- post-firing probability = $6x10^{-3}$

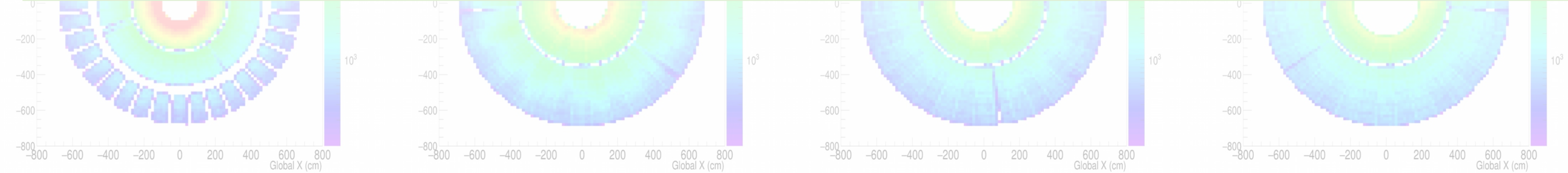
Note: for ME1/3 chambers, Overlap Muon TrackFinder was needed to provide the analysis of the timing

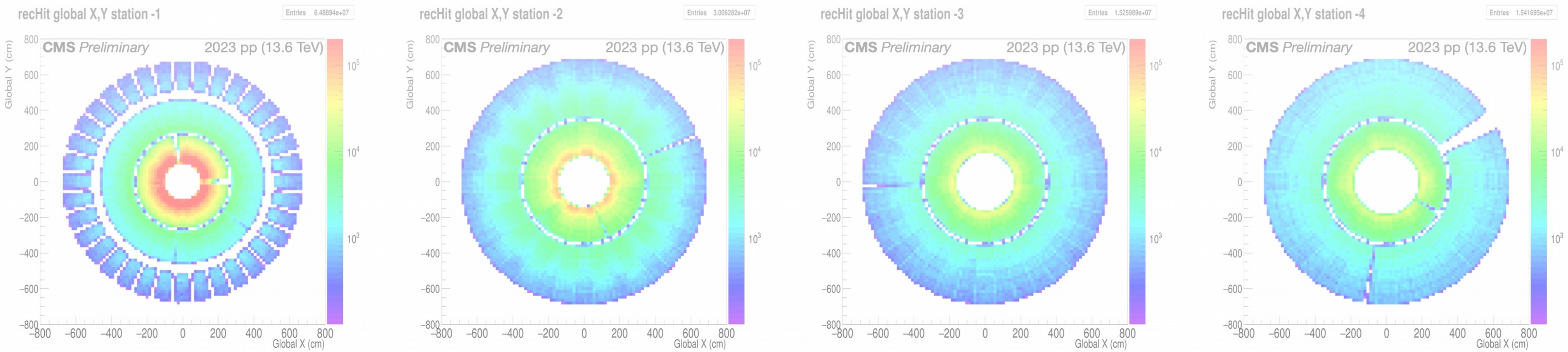
Cathode timing within anode window was also tuned, to guarantee 100% efficiency of readout



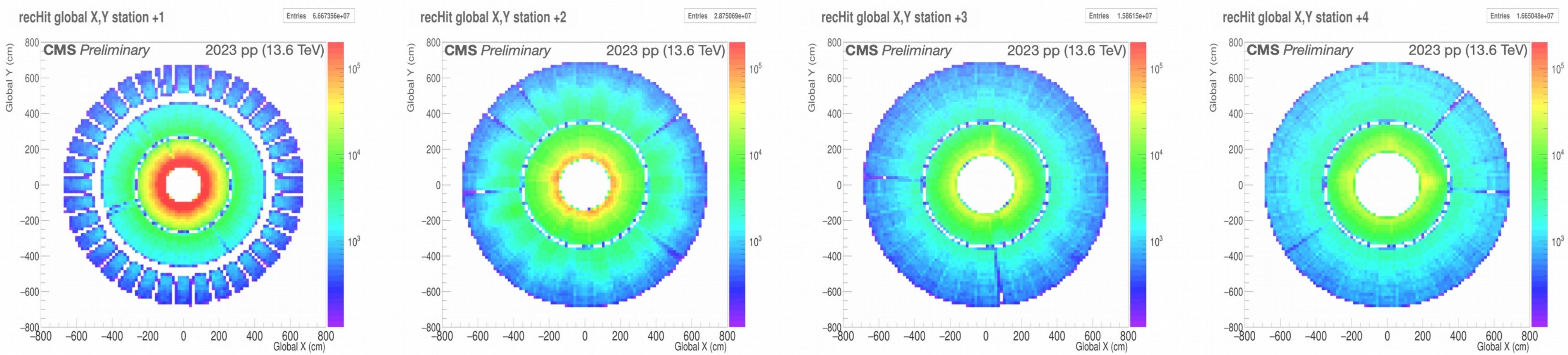


Run 3 Performance (2022 - 2023)



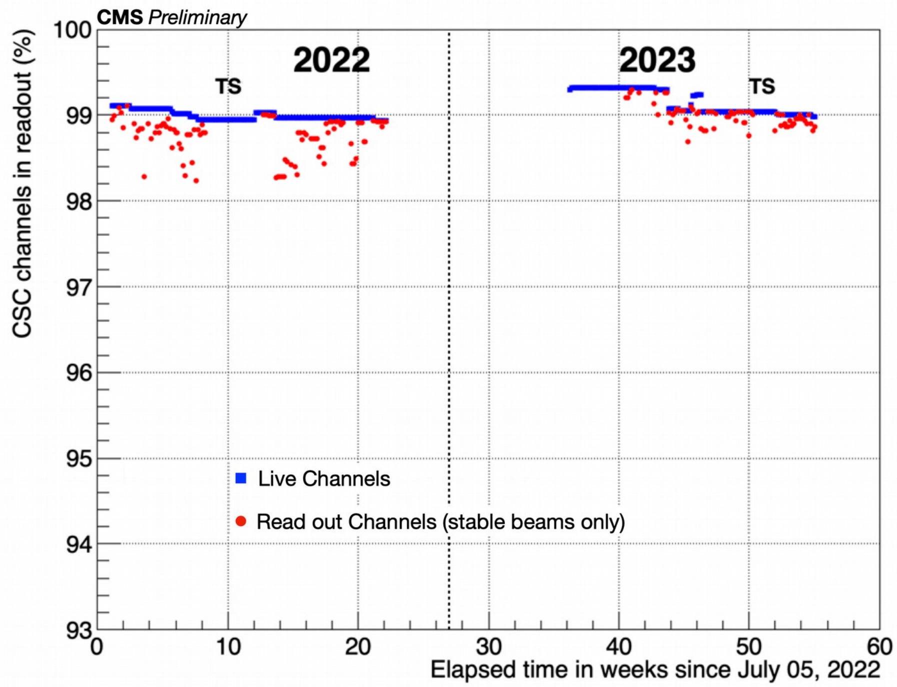


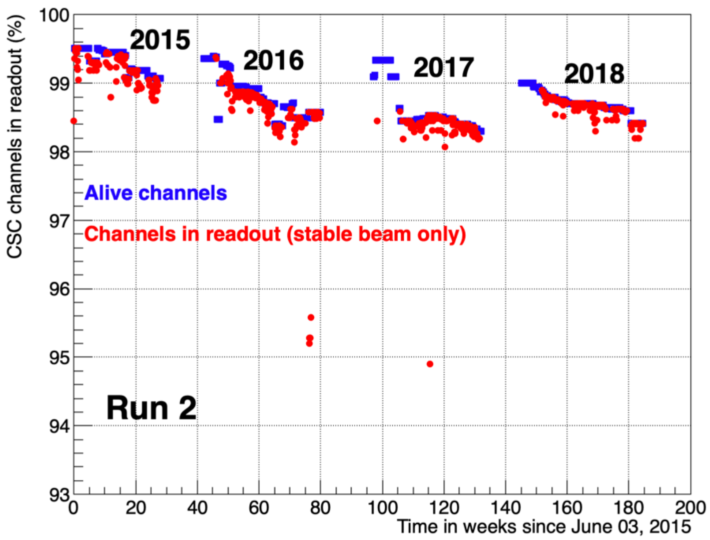
CSC reconstructed hit positions from one run of a muon-triggered dataset



Alive channels

At the end of pp running in July 2023, almost 99% of the electronic channels in the CSC system were live and read out.



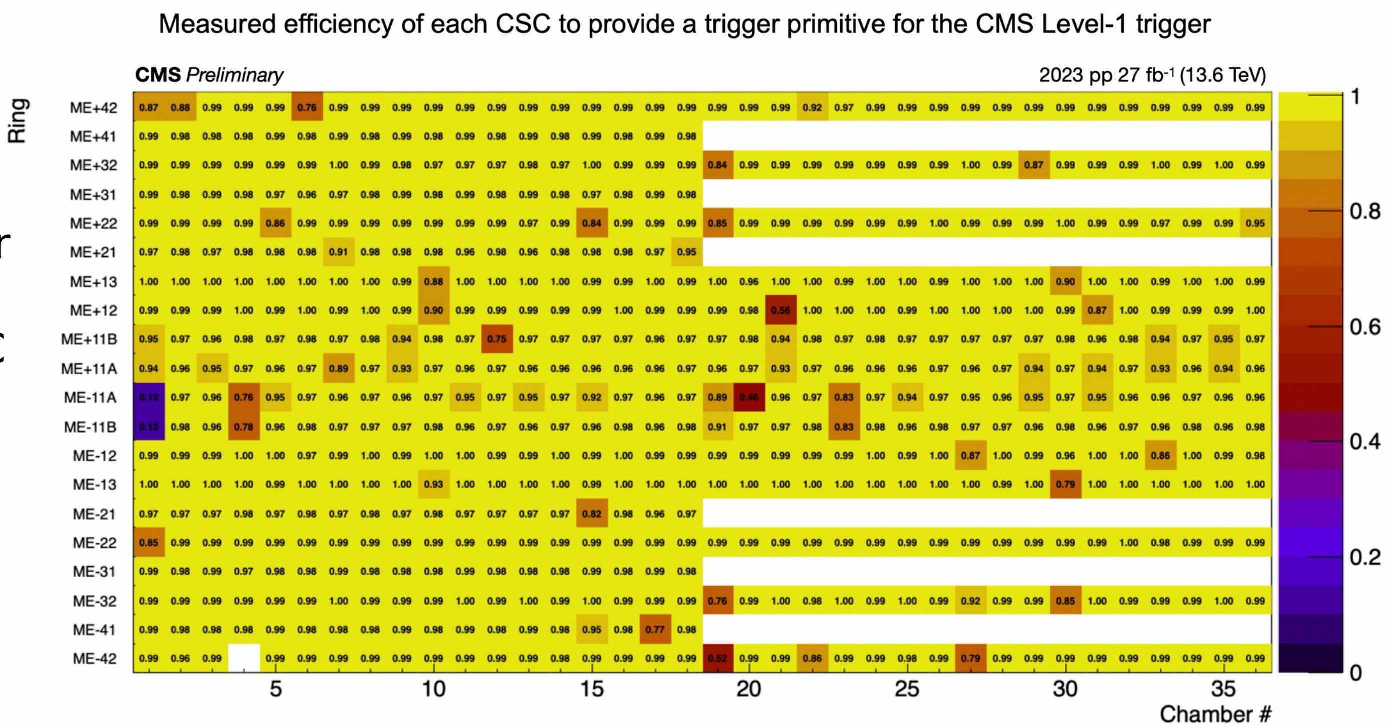


The percentage of active channels in the CSC system, both 'live' (on which electronic signals are produced by the passage of a muon through the system), and 'read out' (which are both live and read out to the CMS DAQ), as a function of time during LHC Run 3 (2022 and 2023).

Trigger Primitive efficiency

The efficiency of each CSC to provide a trigger primitive when a muon passes through the chamber

* More than 98% of the CSC system is operating at close to 100% efficiency.
* The high efficiency and redundant design of the CSC muon detector results in no significant loss in muon trigger and reconstruction efficiency in the endcap region.

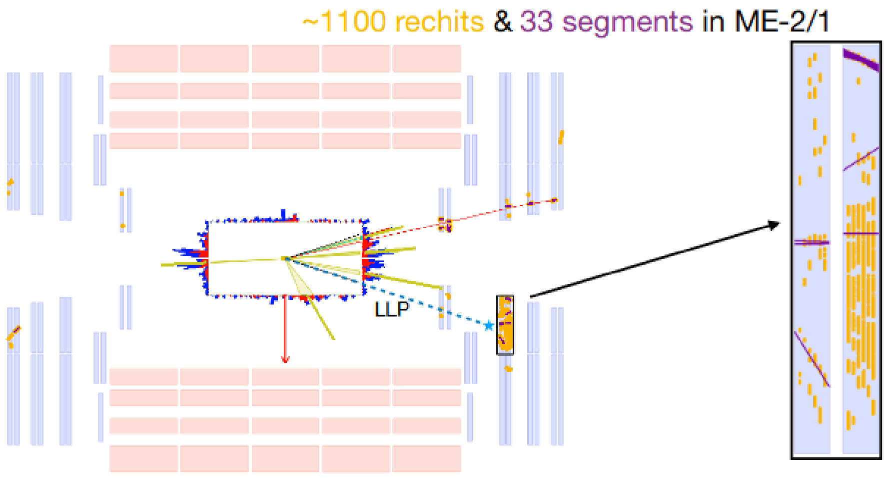


The measured Trigger Primitive efficiency of each of the 540 CSCs in the CMS muon endcap system, labelled by ring, and chamber number within each ring. There are a few chambers with known inefficiency usually due to one or more failed electronics boards which cannot be repaired without major intervention and dismantling of the system. Chamber 4 of ring ME-42 is permanently disabled because of failed electronics which cannot be accessed without dismantling CMS. There are also occasional temporary failures of electronics boards, lasting from periods of hours to days, which can be recovered without major intervention. Both contribute to lowered Trigger Primitive efficiency.

High Multiplicity Trigger

Hadronic shower in the muon system is an unexplored detector signature

- ✶ steel between muon stations can act as absorber, similarly to a sampling calorimeter
- ✶ LLP decaying in the muon system could leave a distinctive high multiplicity signature



Typical example: a scalar particle (Higgs) that decause to 2 LLPs decaying to 2 b-quarks

- ✶ without dedicated trigger: relying on missing energy
- ✶ limited by trigger (MET > 200 GeV)

→ dedicated high multiplicity trigger (HMT) could greatly improve sensitivity

High Multiplicity Trigger

HMT algorithm:

- Count number of hits (single layer!) in cahtodes and anodes of each CSC chamber
- No requirements on patterns
- Require hits in at least 5 out of 6 layers to reduce noise
- Set pre-defined threshold for number of cathode / anode hits per chamber type (location)
- Use an independent trigger path for showers using spare bits

→ Being used in Run 3 (“SingleMuShower” trigger)

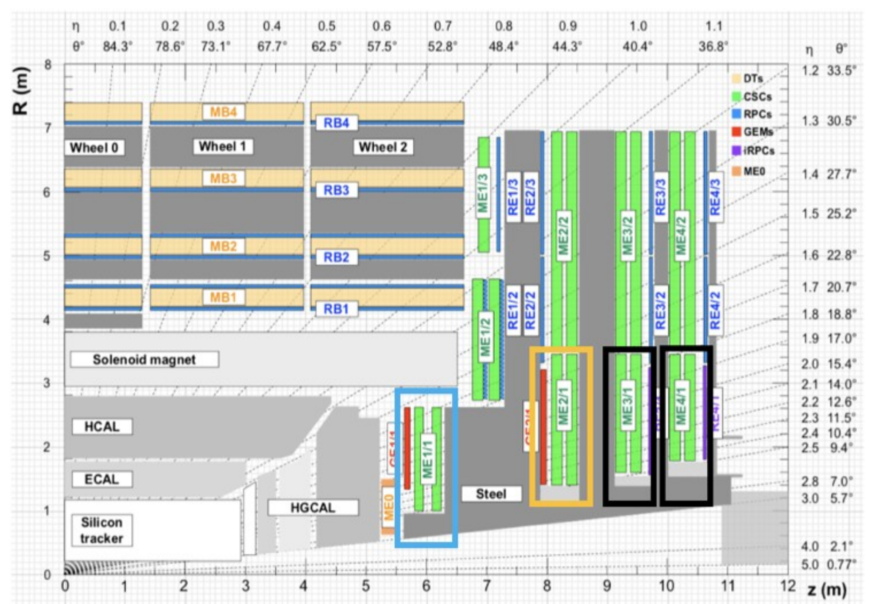
typical thresholds:

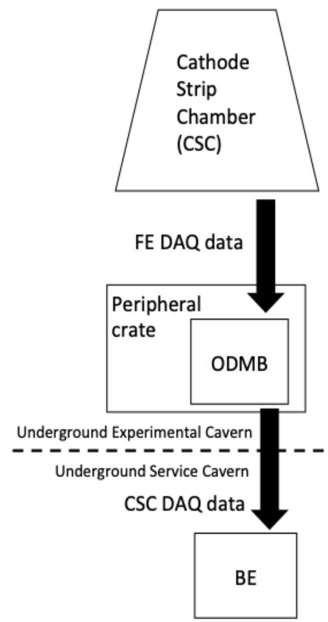
	cathode			anode		
	loose	nominal	tight	loose	nominal	tight
ME1/1	100	100	100	140	140	140
ME1/2	-	-	-	140	140	140
ME1/3	-	-	-	7	14	18
ME2/1	14	33	35	23	56	58
ME2/2	-	-	-	12	28	32
ME3/1	12	31	33	21	55	57
ME3/2	-	-	-	12	26	34
ME4/1	14	34	36	25	62	64
ME4/2	-	-	-	12	27	31

LS3 Upgrade (2026 - 2028)

Remaining CSC Upgrade for HL-LHC

- ✶ The Optical Data MotherBoards (ODMBs) are VME boards that read out the CSC chambers
- ✶ Legacy ODMBs were installed in 2013 in ME1/1 and have worked extremely well
- ✶ To meet bandwidth requirements for HL-LHC, 2 new versions of the ODMB are being developed: ODMB7 (to read out ME1/1 chambers) and ODMB5 (to read out ME2/1, ME3/1, and ME4/1)
- ✶ In addition, the backend will be replaced for the full CSC system, using a modular ATCA card





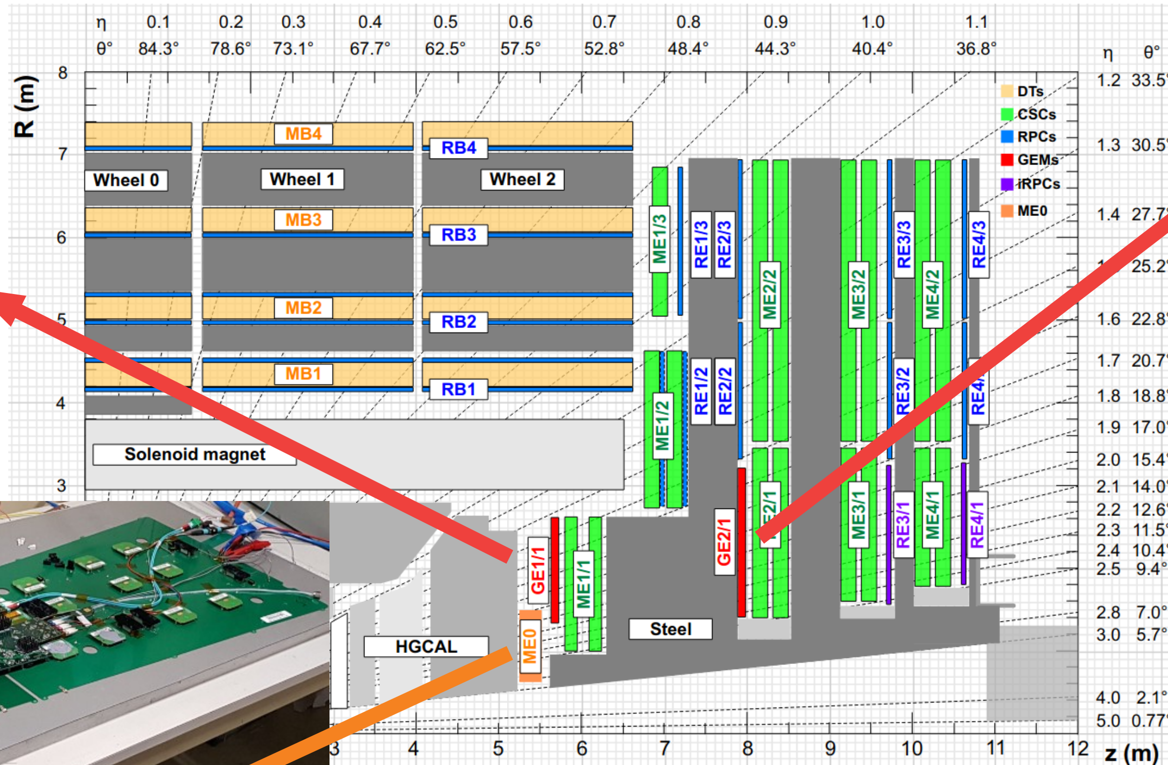
UCSB graduate students installing ODMBs in a peripheral crate under CMS in 2013.

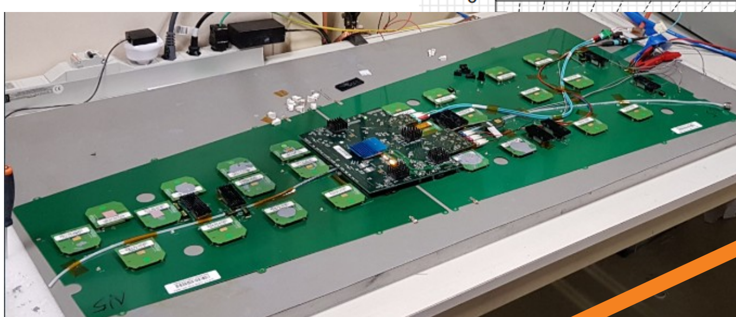
The GEM–CSC Trigger

CMS GEM Detectors

GE1/1:

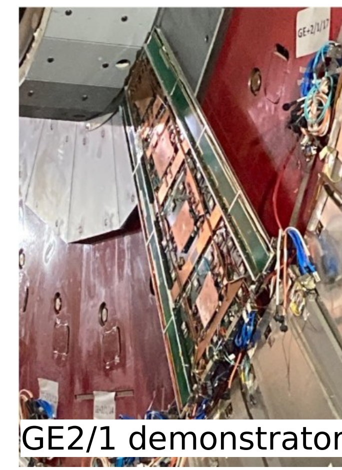
- ✶ installed during LS2
- ✶ 2 detection layers in front of ME1/1 CSC chambers





GE2/1:

- ✶ 2 detection layers in front of ME2/1 CSC chambers

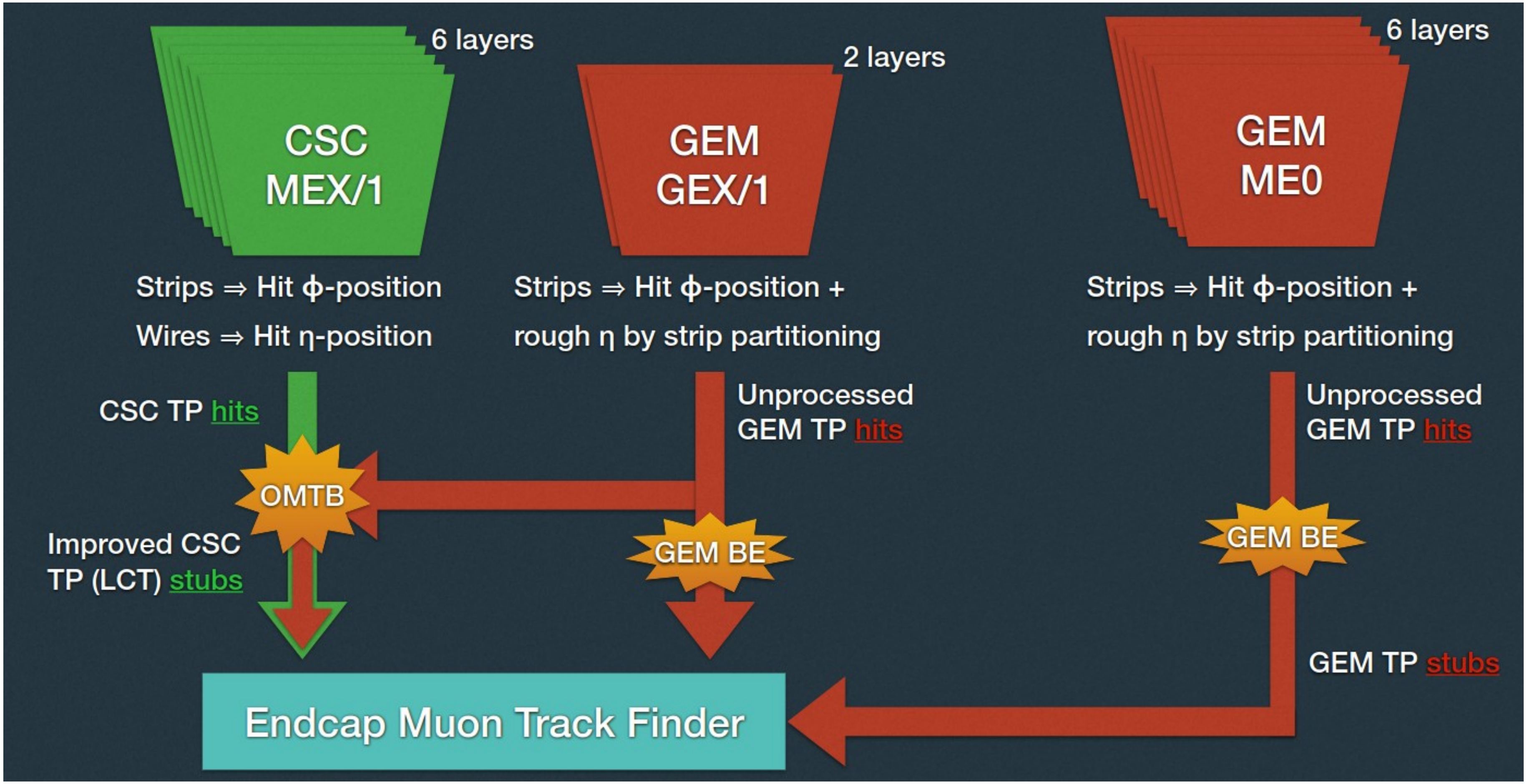


GE2/1 demonstrator

ME0:

- ✶ 6 layers
- ✶ extend coverage to 2.4 < |η| < 2.8

GEM in L1 Trigger



GEM–CSC Trigger

More robust primitives with CSC and GEM information at OTMB level:

- ✶ Receive GEM trigger clusters, in addition to standard CSC Local Charged Tracks (LCTs)
- ✶ Build 2-layer coincidence with GEM clusters
- ✶ Convert GEM cluster coordinates into CSC coordinates + match with CSC ALCTs (wires) and CLCTs (strips) in time & position
- ✶ Build up to 2 LCT (CSC+GEM) per BX

Match Type	Timing	Anode Position	Cathode Position	bending	Quality
ALCT-CLCT-Copad	ALCT	ALCT WG	CLCT HS	GEM-CSC	111
				CSC-only	110
ALCT-CLCT-1GEM	ALCT	ALCT WG	CLCT HS	GEM-CSC	101
				CSC-only	100
ALCT-CLCT	ALCT	ALCT WG	CLCT HS	CSC only	011
CLCT-Copad	GEM	GEM roll	CLCT HS	GEM-CSC	001
ALCT-Copad	ALCT	ALCT WG	GEM pad	GEM only	010


Backup

Chamber parameters

Parameter	ME1/1	ME1/2	ME1/3	ME2/1	ME3/1	ME4/1	ME234/2
Basic single plane parameters							
full gas gap (2h), mm	6			9.5			
wire diameter, μm	30			50			
wire spacing, mm	2.5	3.16	3.16	3.12	3.12	3.12	3.16
Active area							
width (top), mm	487	819	933	1254	1254	1254	1270
width (bottom), mm	201	511	630	534	617	685	666
length, mm	1505	1635	1735	1900	1680	1500	3215
Wires							
wire tilt	25°			0°			
wires per plane	600	528	560	620	550	492	1028
wires per wire group	11-12	11	12	5, 6	5, 6	5	16
wire group width, mm	27.5-30	35	38	16, 19	16, 19	16	51
wire group cap., pF	60-150	40-70	50-80	20-60	20-60	25-45	80-150
wire channels per plane	48	48	48	112	96	96	64
Strips							
Δφ(single strip), mrad	2.96	2.33	2.16	4.65	4.65	4.65	2.33
width (top), mm	7.6	10.4	14.9	15.6	15.6	15.6	16.0
width (bottom), mm	3.15	6.6	11.1	6.8	7.8	8.6	8.5
gap between strips, mm	0.35			0.5			
strip capacitance, pF	90-140	110	145	145	130	120	250
radial split of strips	@η=2.0			none			
strip channels per plane	2x64	80	64	80	80	80	80

Parameter	ME1/1	ME1/2	ME1/3	ME2/1	ME3/1	ME4/1	ME234/2
HV							
Operating HV [kV]	~3.0			4.1			
HV segments per plane	1 or 2	2	3	3	3	3	5
Overall chamber parameters							
Number of chambers	72	72	72	36	36	36	216
Planes/chamber				6			
φ-coverage, degrees	10°	10°	10°	20°	20°	20°	10°
φ-overlap, strips	5	5	none	5	5	5	5
η-coverage	1.5-2.4	1.2-1.6	0.9-1.1	1.6-2.4	1.75-2.4	1.85-2.4	varies
η-overlap				none			
Length, mm	1680	1800	1900	2065	1845	1665	3380
Width (top), mm	613	1078	1192	1534	1534	1534	1530
Width (bottom), mm	311	740	859	751	835	903	895
Chamber thickness, mm	148			250			
Chamber weight, kg	~60	150	160	190	180	160	276

- Parameters from Muon TDR (1997)
  - http://cds.cern.ch/record/343814

Gas gap: 6 - 9.5 mm
Wire spacing: 2.5 - 3.16 mm
Strip width: 3.15 - 16 mm

Some of these different in final design, eg. HV

Manuel Franco Sevilla   Introduction to the CSC system   **Slide 21**

ME234/1 Phase-2 Upgrade

LS2

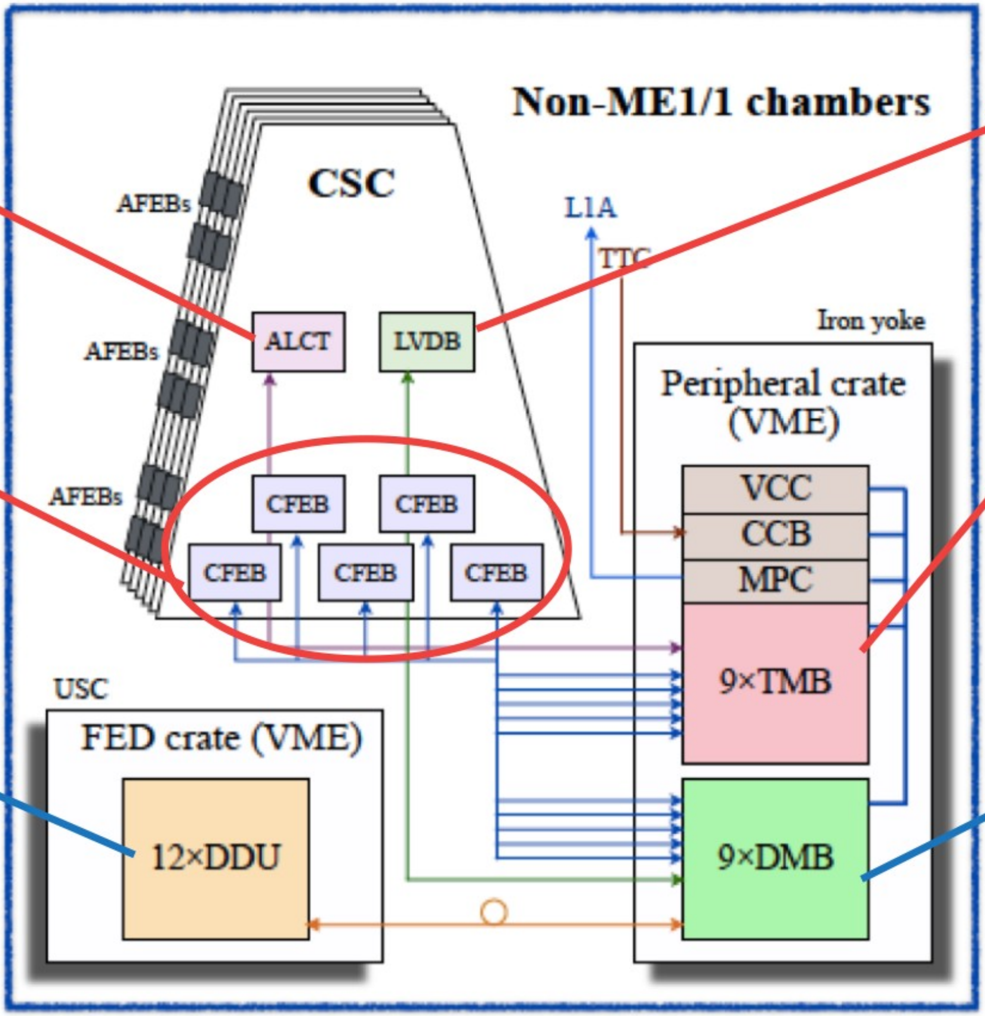
Anode Local Charged Track electronics: replace mezzanine cards to increase latency capability and output bandwidth

LS2

Cathode Front End Boards: replace with Digital Cathode Front End Boards with increased latency and rate capabilities

LS3

Front End Driver: increased data volume, number of links



LS2

Low Voltage Distribution Boards: replace to provide voltages and currents for Digital Cathode Front End Boards

LS2

Trigger Motherboard: replace with optical Trigger Motherboard to receive Digital Cathode Front End Board trigger data, increased algorithmic power

LS3

Data Motherboard: replace with optical Data Motherboard to receive Digital Cathode Front End Board data

ME1/1 Phase-2 Upgrade

- New version of DCFEBs installed on ME1/1 (xDCFEBs)
  - featuring remote programming of FPGA (via GBTx) to provide an alternative to programming via on-board EEPROM after experiencing instances of EEPROM corruption in 2017
- ME1/1 DCFEBs were installed on ME234/1
  - dose rate almost 1 order of magnitude lower than in ME1/1
  - optical transmission consolidation because of 3-4% transceiver (Finisar) failure rate in 2016-2018
    → VTTx+adapter board