# Trigger and Data Acquisition
## at colliders

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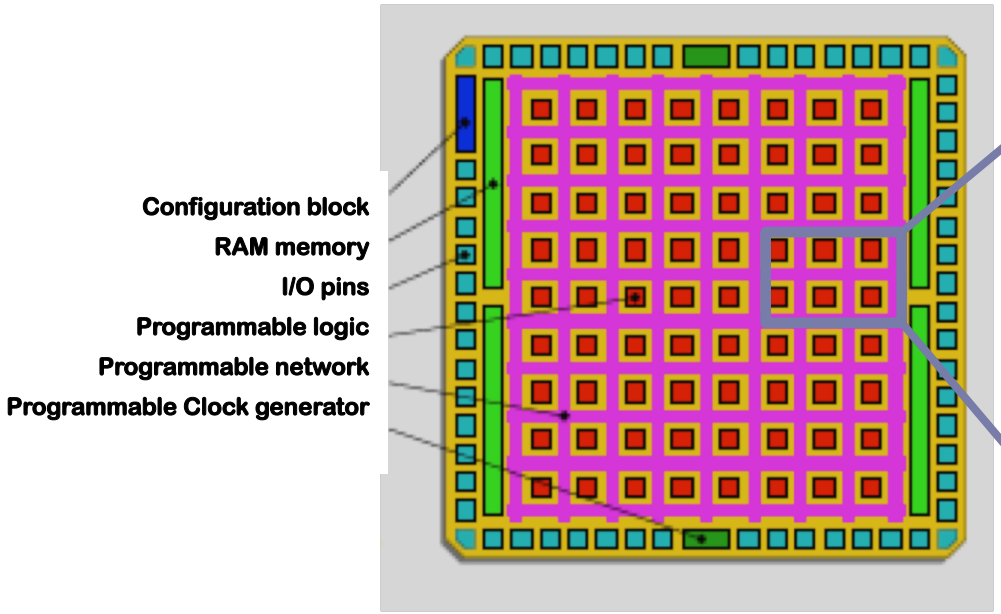
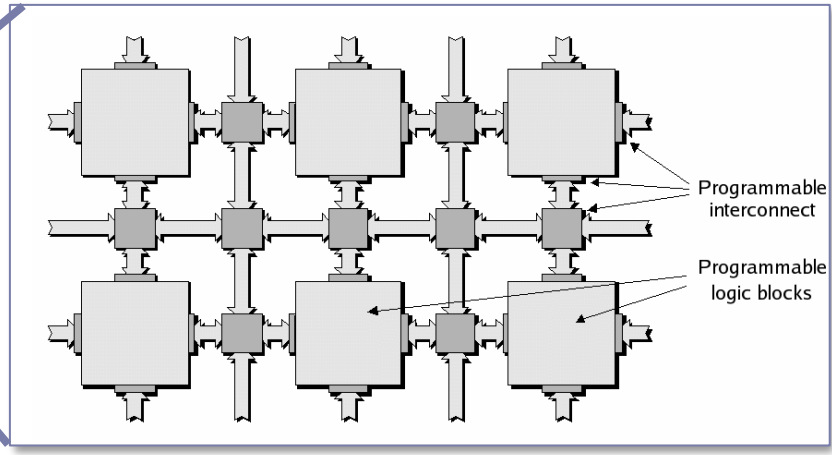
# MORE ON FPGA

# Introduction

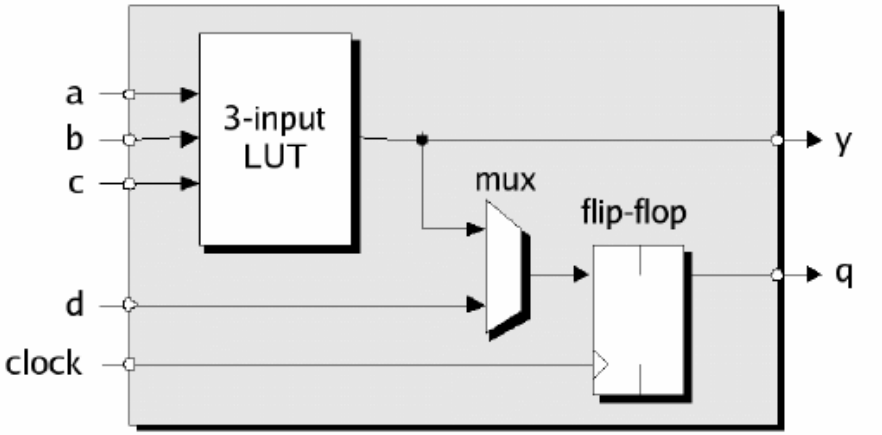
- Field Programmable Gate Array
  - *A dense array of Programmable logic blocks (PLB), connected via programmable interconnects*
  - *+ RAM memories*
  - *+ clock*
  - *+ I/O*



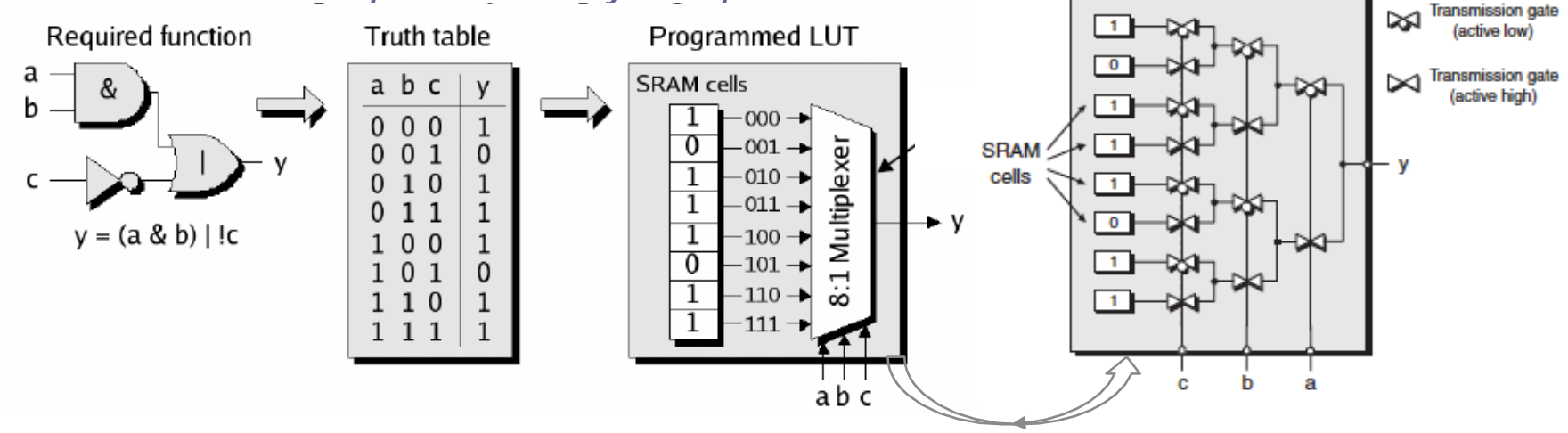
# Inside the FPGA

- Typical FPGA Programmable Logic Block
  - *3-input lookup table (LUT), a register (flip-flop) and a MUX*

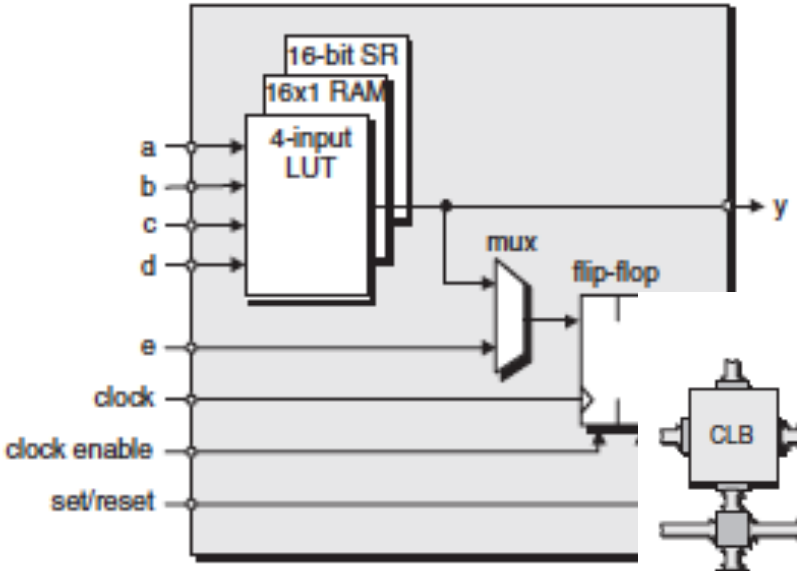




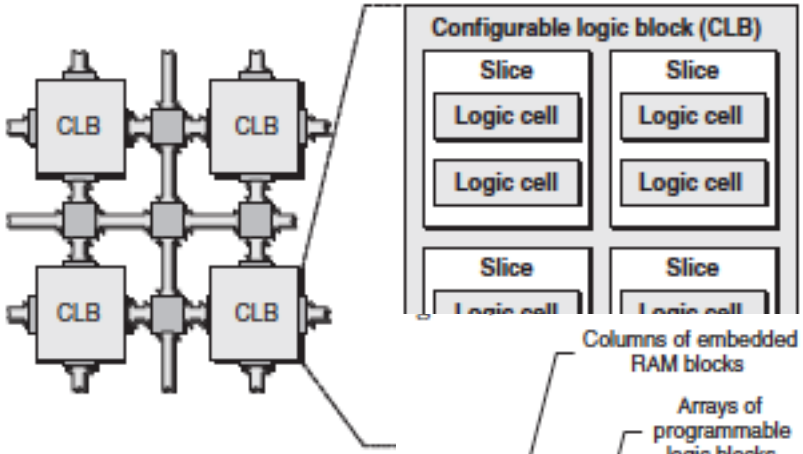

  - *The LUT can implement any 3-input function*

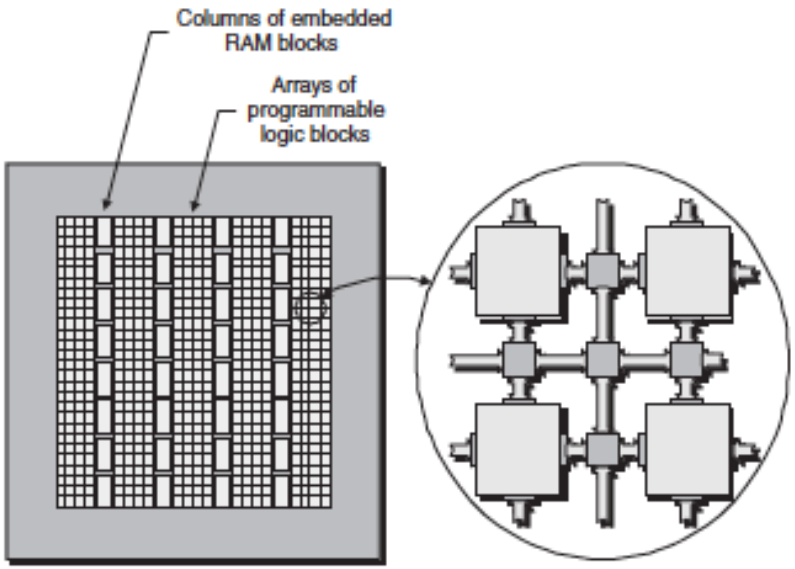


# In reality




**Configurable Logic Cell Block**
**4-input LUT + RAM + Shift Register**




**+ Clock distribution Tree**
**+ numerous I/O**
**+ several Gigabit transceivers**

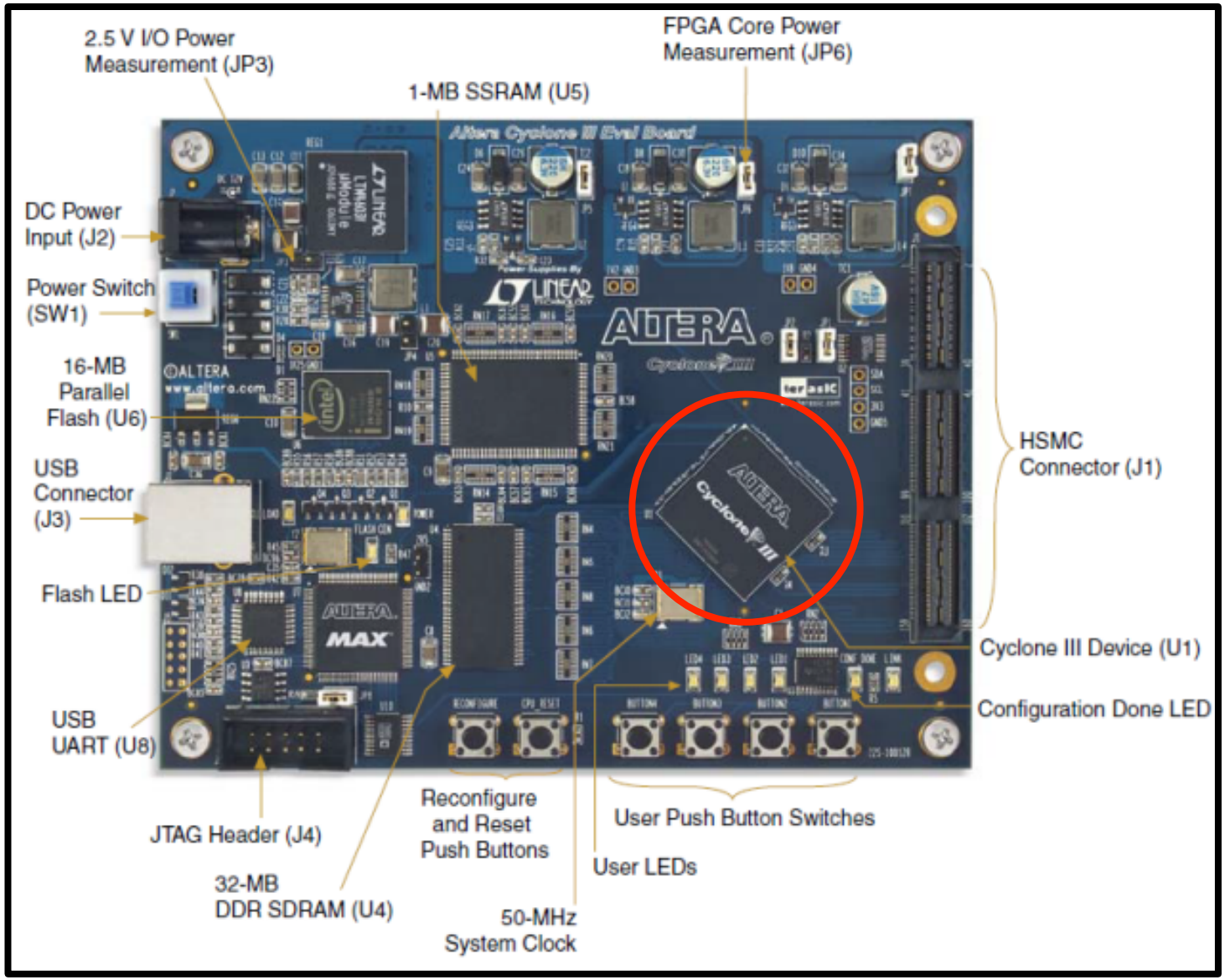
# Today's FPGAs

- Up 2 millions of logic cells
- Several hundreds of general purpose I/O's
- 10 Gb/s – 28 Gb/s high speed serial transceivers
- You can program Soft-core CPUs (and program in C)

# INTRODUCTORY PART FOR THE LAB SESSION

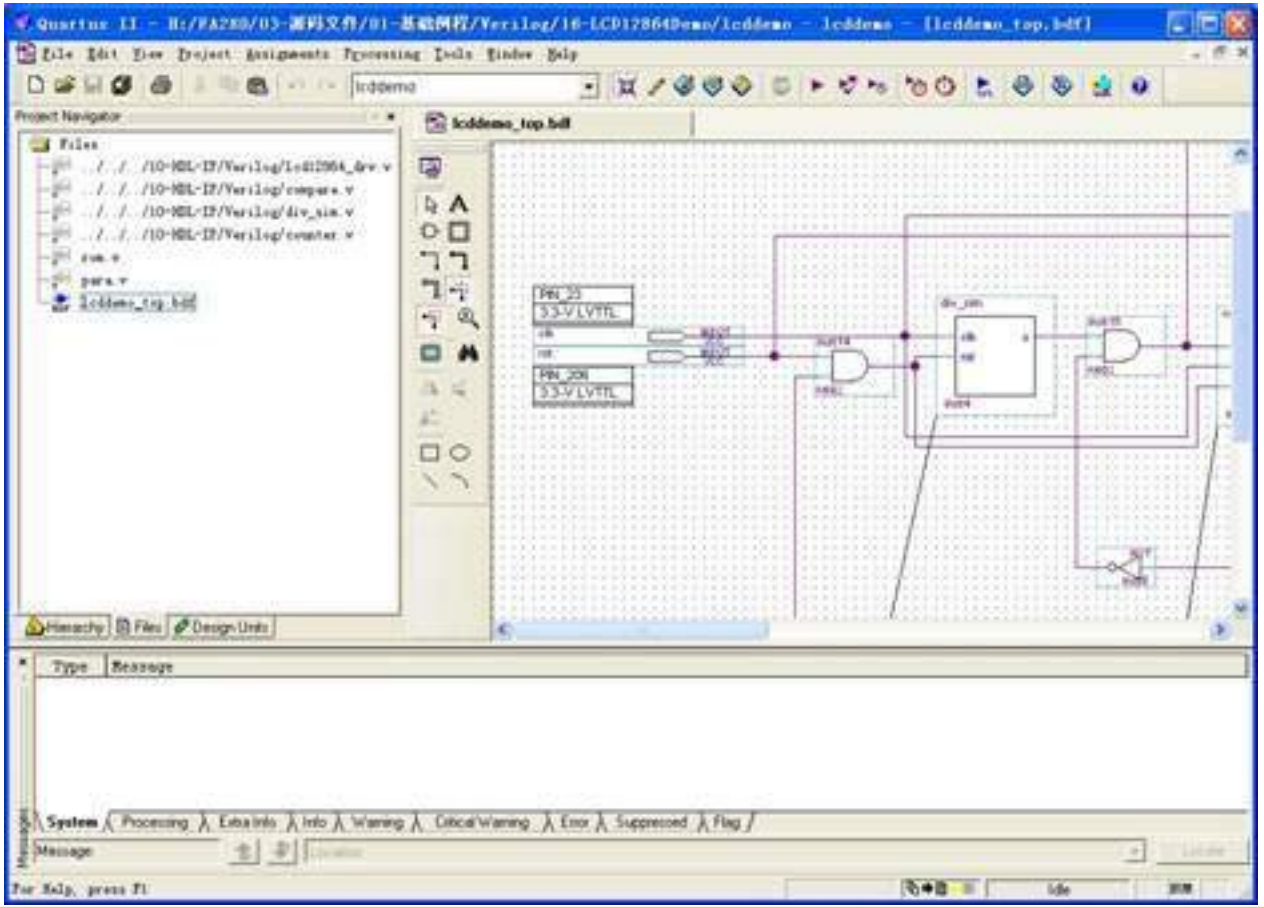
# The HW equipment

- FPGA ALTERA Cyclone III dev. board + extension board to send/read signals



# Software

- Quartus II (Linux/Windows)
  - *Fully integrated design entry methods*
  - *Logic synthesis, Place and route*
  - *Device programming*
  - *+ simulations*
  - *Timing analysis*
  - *…*

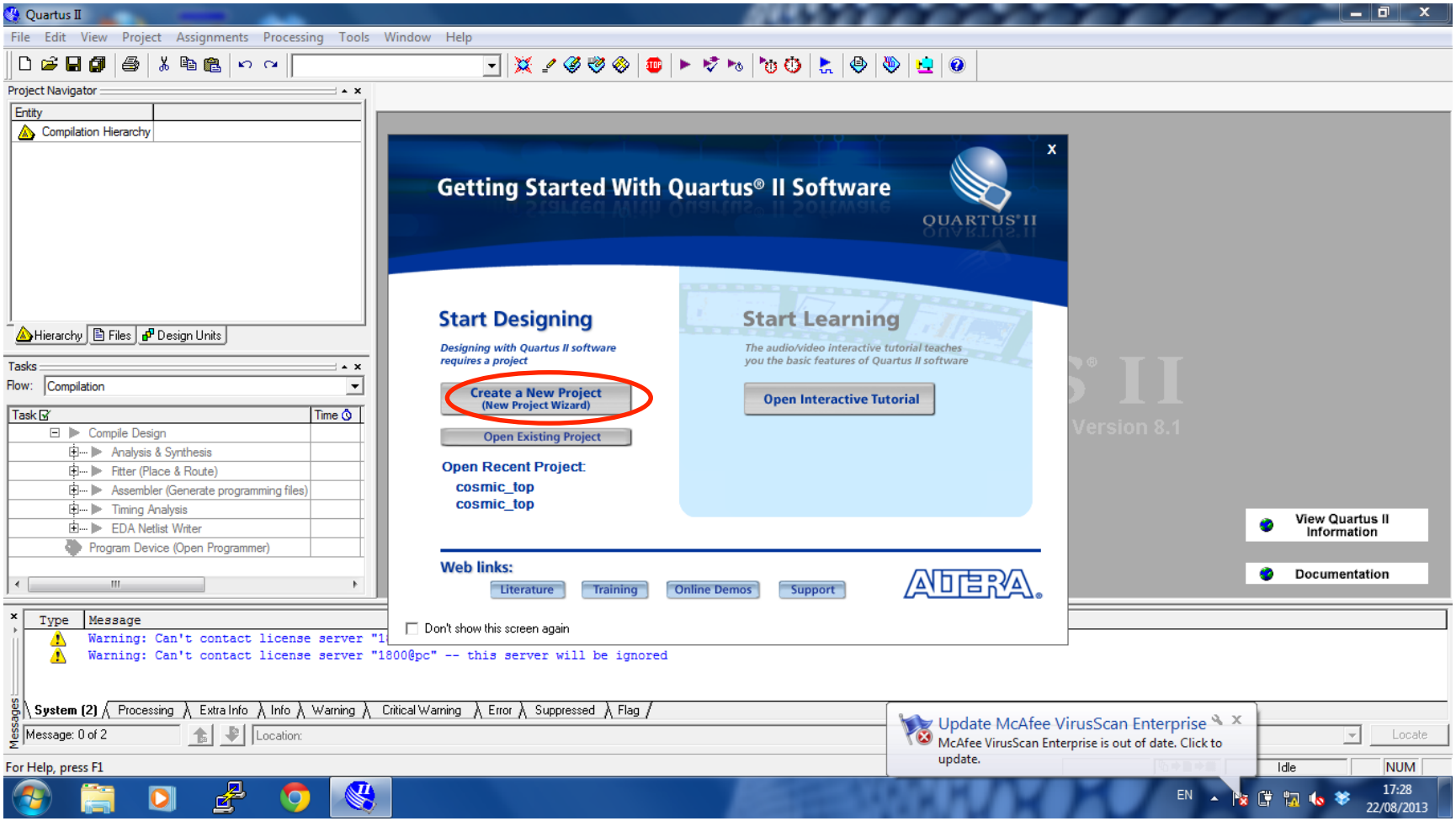


# Your First FPGA Design Tutorial

- Task 1:
  - *Create a design that causes LEDs on the development board to blink at a speed that is controlled by an input button*
- Task 2:
  - *Route clock signals to general I/O pins and use the extension board to send the signals to an oscilloscope*
- Task 3:
  - *use external clock generator to drive the LEDs*
- You will write code in Verilog Hardware Description Language as well as use the schematic interface
  - *No knowledge of Verilog is needed; the code will be provided and explained.*

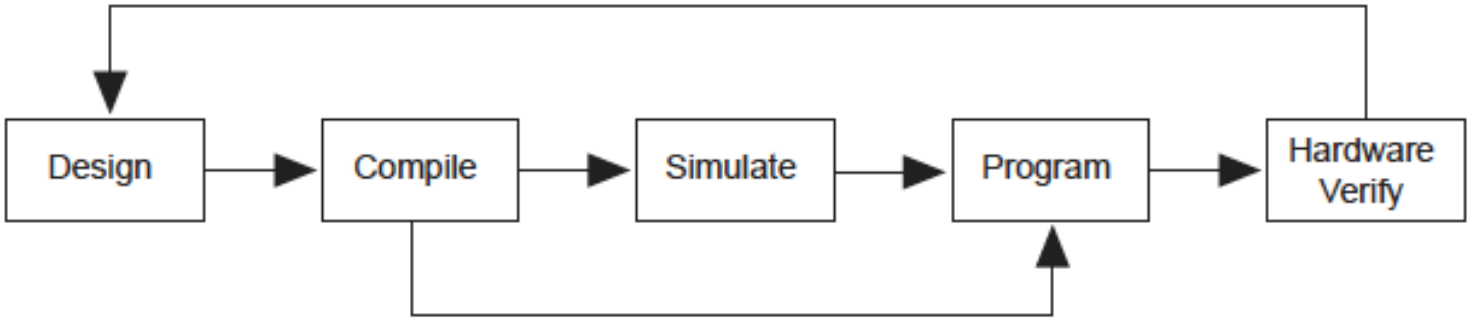
# The tutorial in 5 slides

- You will receive the full tutorial at the lab session
- Launch Quartus II:



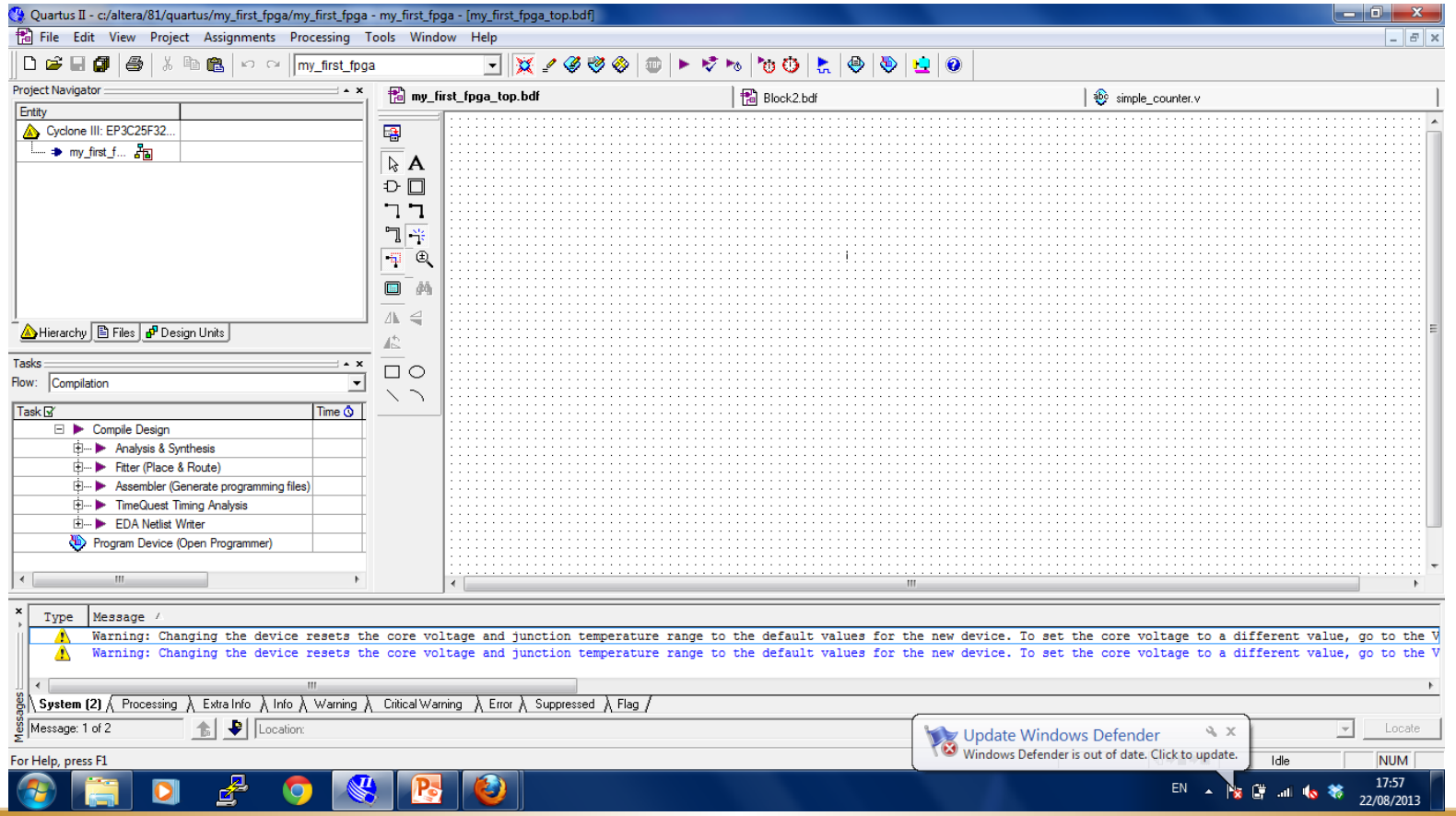
# The tutorial in 5 slides

- The design flow:



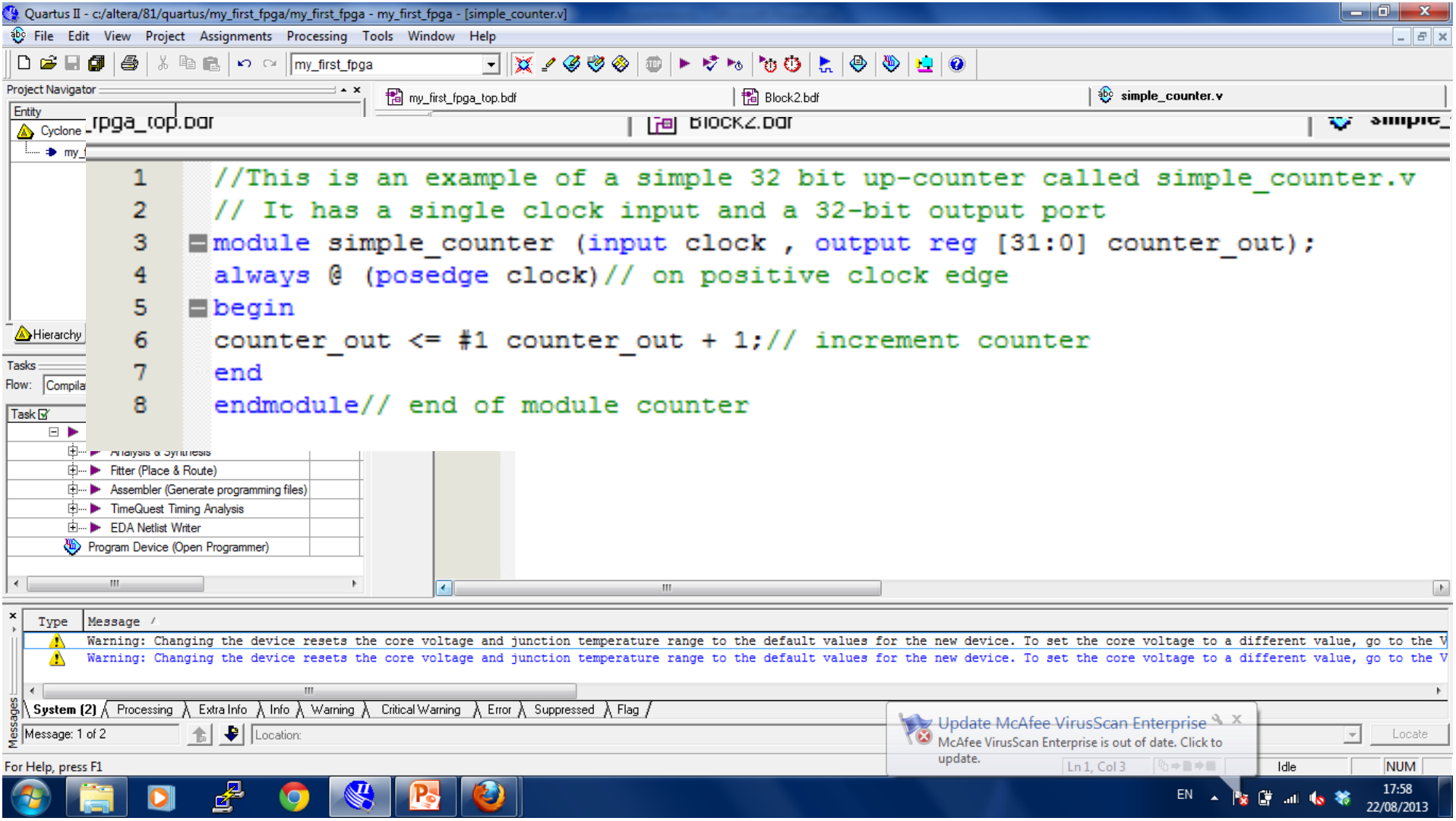
# The tutorial in 5 slides

- The design should match the hardware !
- The development board is equipped with a Cyclone III FPGA
  - *Name: EP3C25F324C6*
- Empty working area:



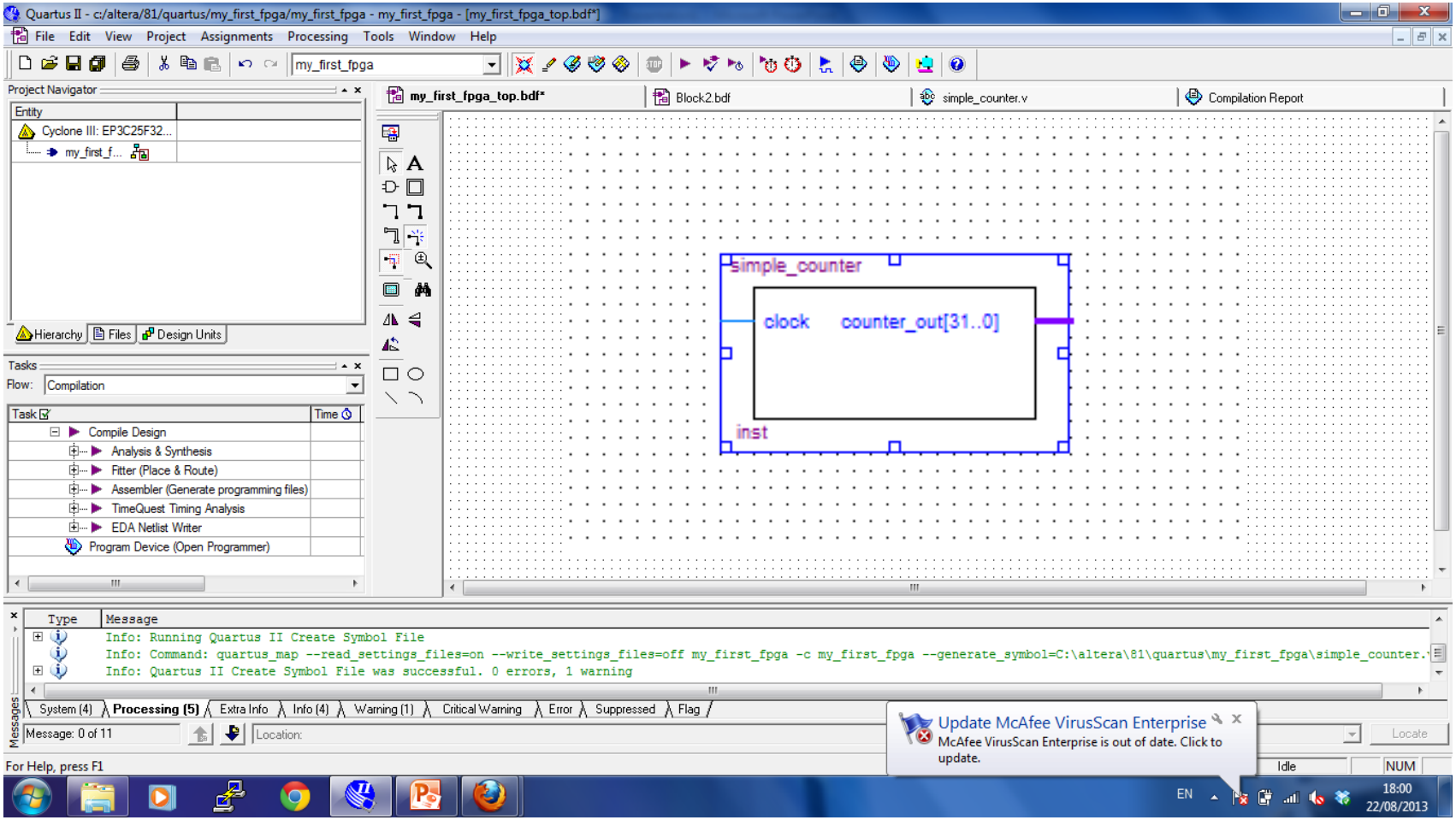
# The tutorial in 5 slides

- Write a first Verilog code to create a counter



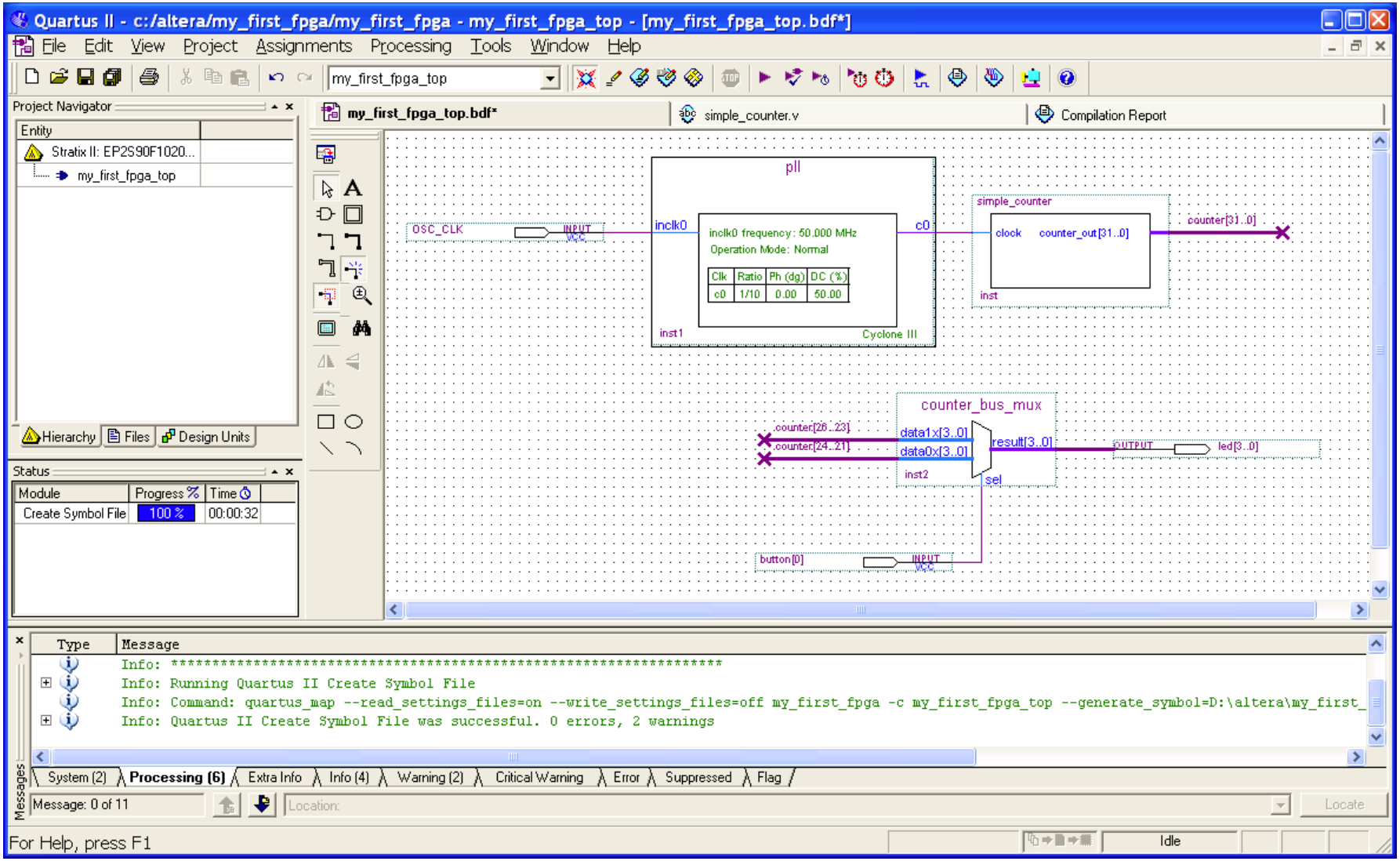
# The tutorial in 5 slides

- Make from this counter a schematic object:



# The tutorial in 5 slides

- After some steps:



# The tutorial in 5 slides

- Last steps:
  - *Assign the pins (to effectively connect in the hardware the FPGA to the other devices – clock, button, GPIOs, etc.)*
  - *Compile the your project*
  - *Program the FPGA (through the USB interface)*
  - *Run the program in FPGA hardware*

# References & practical infos

- ALTERA
  - *http://www.altera.com/*
- My First FPGA Design
  - *http://www.altera.com.cn/literature/tt/tt_my_first_fpga.pdf*
- The Design Warrior's Guide to FPGAs: Devices, Tools and Flows
  - *C. Maxfield, ISBN 0750676043*
- Note : we could have done the same with Xilinx FPGAs ;-)
  - *http://www.xilinx.com/*
- For the lab sessions:
  - *Each group of students will have 1 FPGA board, 1 oscillo and notes*
  - *We have Windows laptops, but you could also do it on your laptop*
    - Install before the lab quartus II web edition

    http://www.altera.com/products/software/quartus-ii/web-edition/qts-we-index.html