

# Trigger and Data Acquisition at colliders

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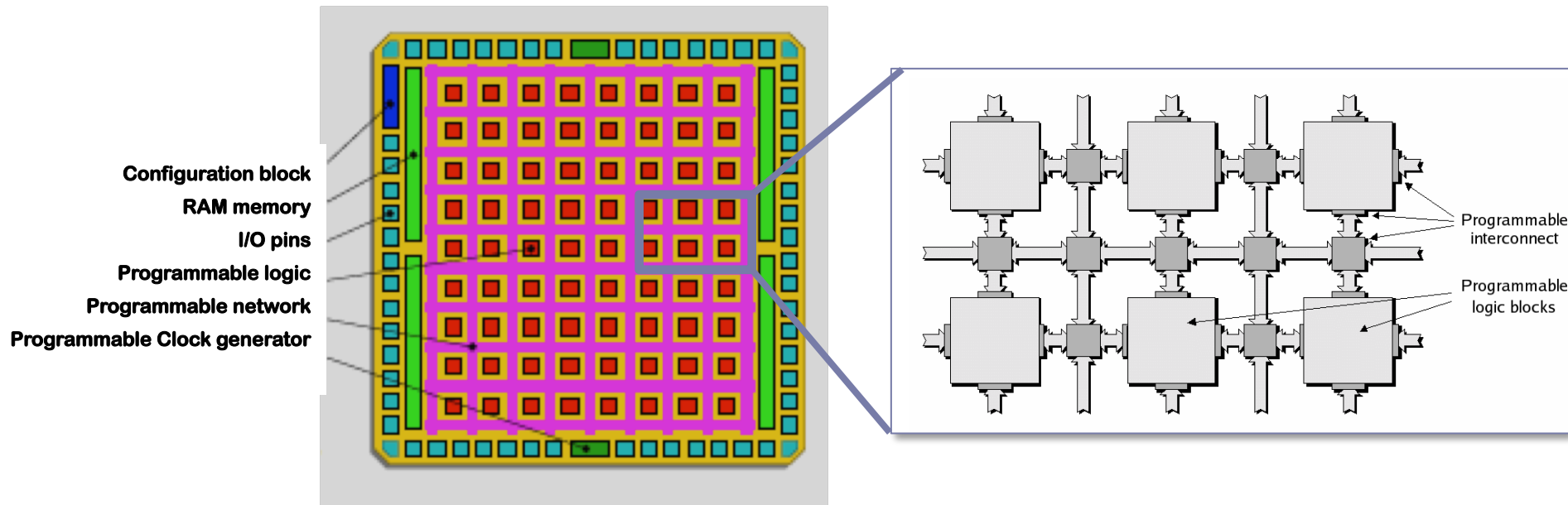
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# MORE ON FPGA

# Introduction

## Field Programmable Gate Array

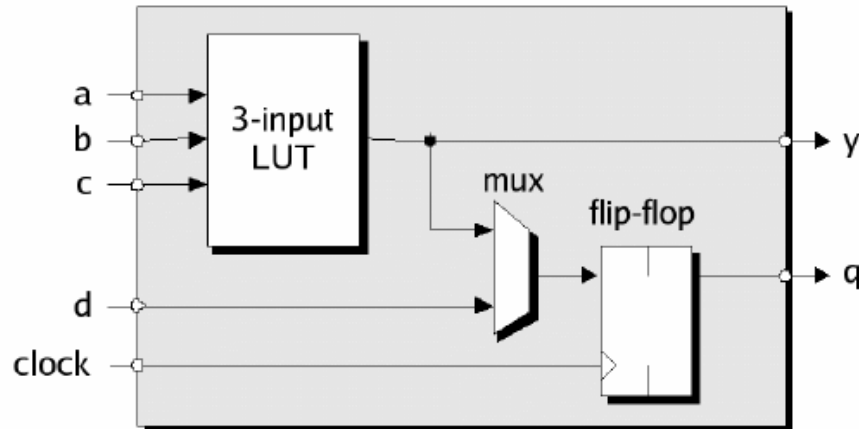
- *A dense array of Programmable logic blocks (PLB), connected via programmable interconnects*
- *+ RAM memories*
- *+ clock*
- *+ I/O*



# Inside the FPGA

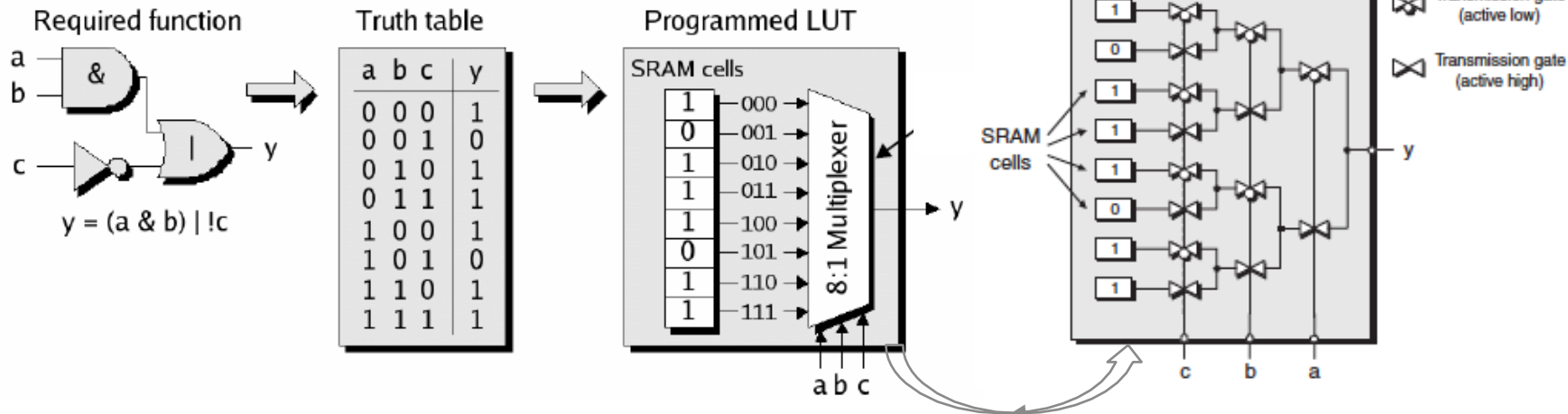
## Typical FPGA Programmable Logic Block

- 3-input lookup table (LUT), a register (flip-flop) and a MUX

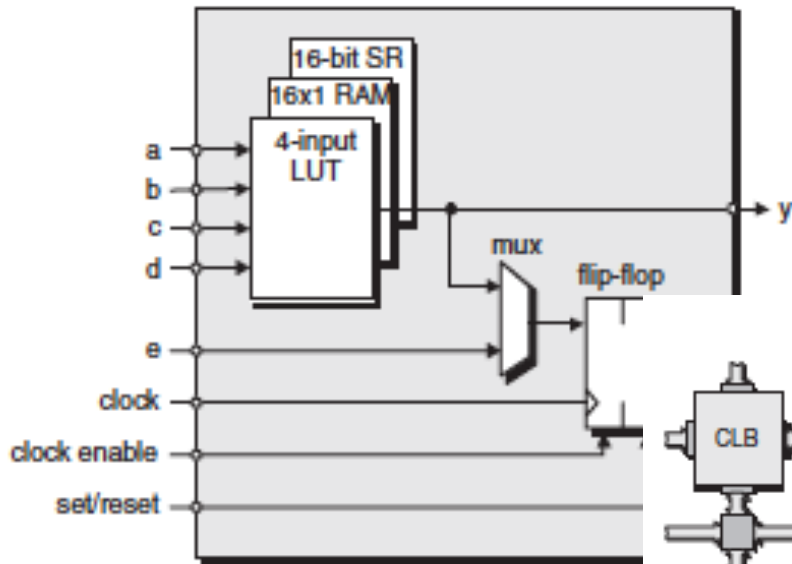


The Design Warrior's Guide to FPGAs,  
ISBN 0750676043,  
Copyright(C) 2004 Mentor Graphics Corp

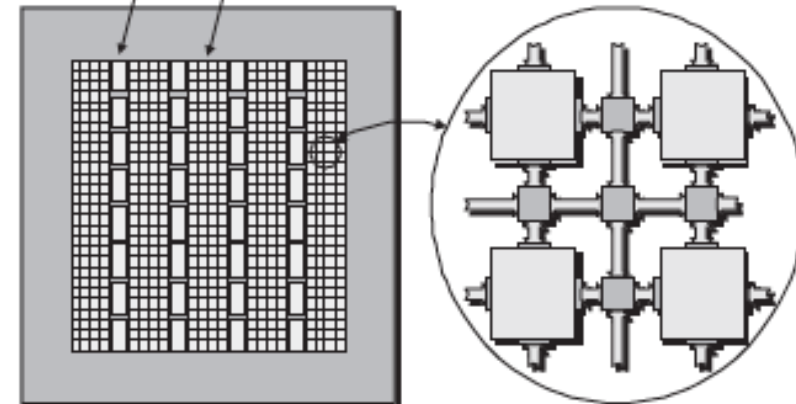
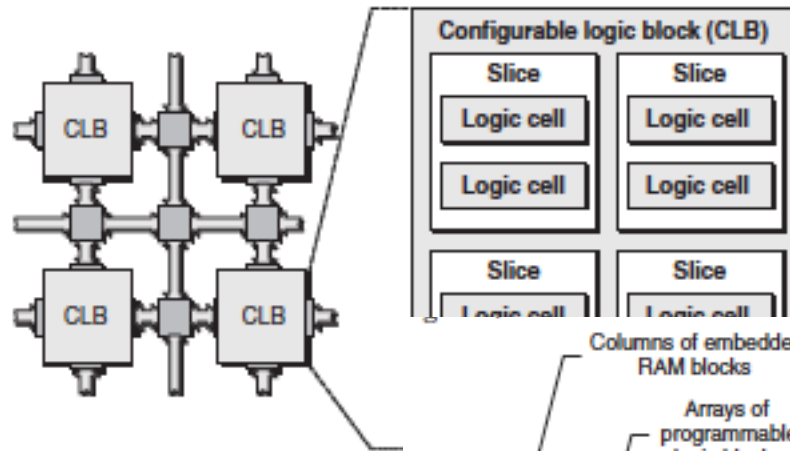
- The LUT can implement any 3-input function



# In reality



**Configurable Logic Cell Block**  
**4-input LUT + RAM + Shift Register**



- + Clock distribution Tree
- + numerous I/O
- + several Gigabit transceivers

# Today's FPGAs

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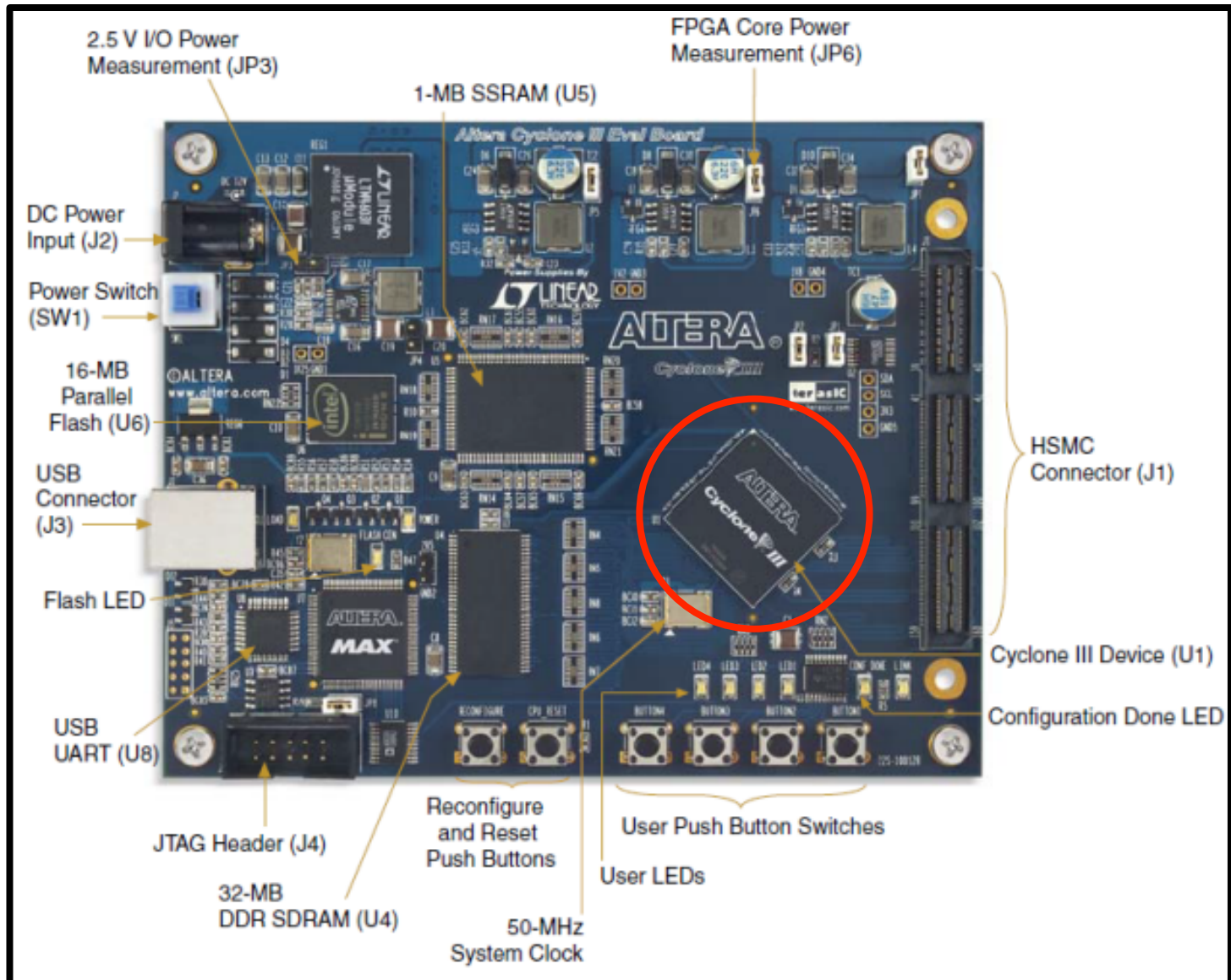
- Up 2 millions of logic cells
- Several hundreds of general purpose I/O's
- 10 Gb/s – 28 Gb/s high speed serial transceivers
- You can program Soft-core CPUs (and program in C)

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# **INTRODUCTORY PART FOR THE LAB SESSION**

# The HW equipment

- FPGA ALTERA Cyclone III dev. board + extension board to send/read signals

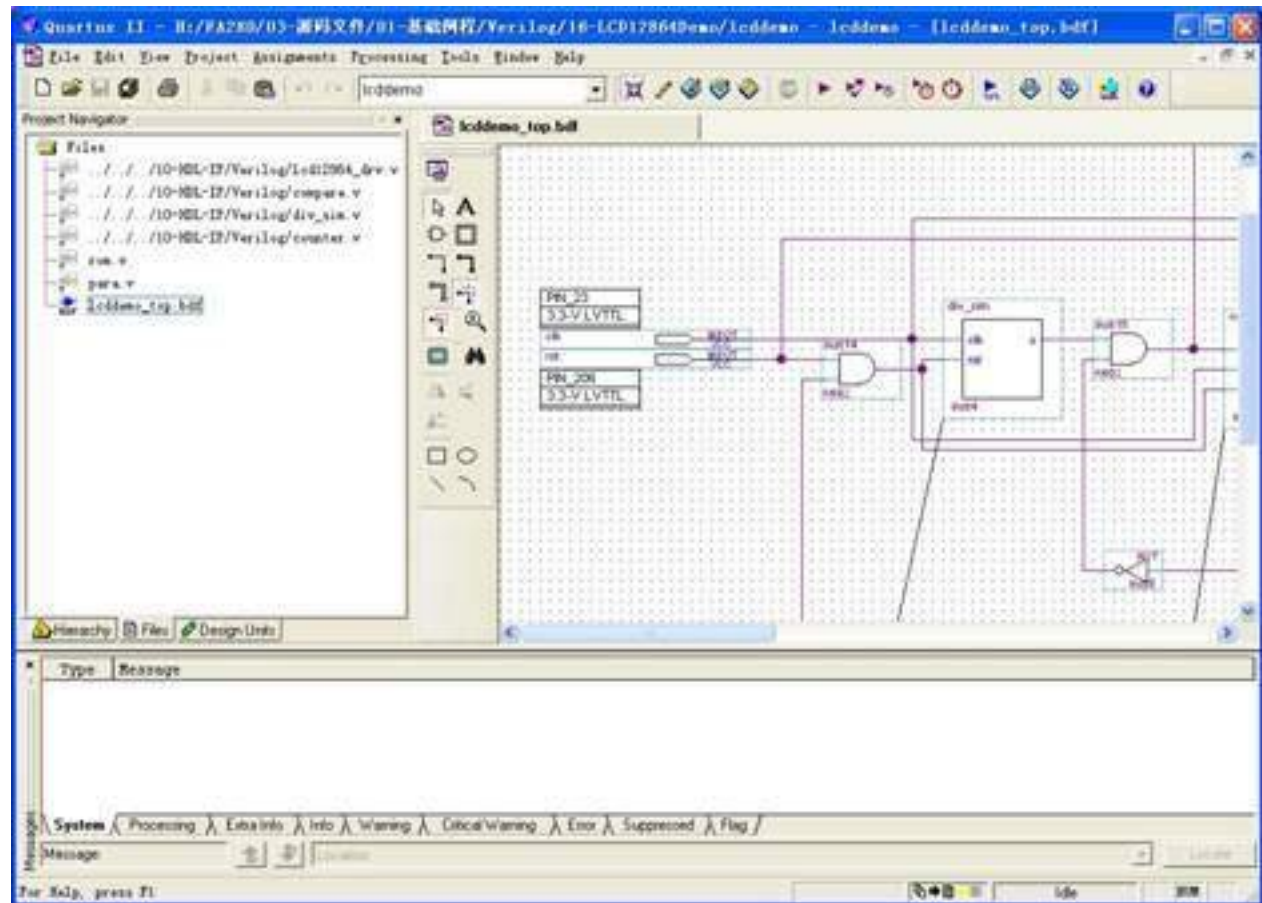




# Software

## Quartus II (Linux/Windows)

- Fully integrated design entry methods
- Logic synthesis, Place and route
- Device programming
- + simulations
- Timing analysis
- ...



# Your First FPGA Design Tutorial

## Task 1:

- *Create a design that causes LEDs on the development board to blink at a speed that is controlled by an input button*

## Task 2:

- *Route clock signals to general I/O pins and use the extension board to send the signals to an oscilloscope*

## Task 3:

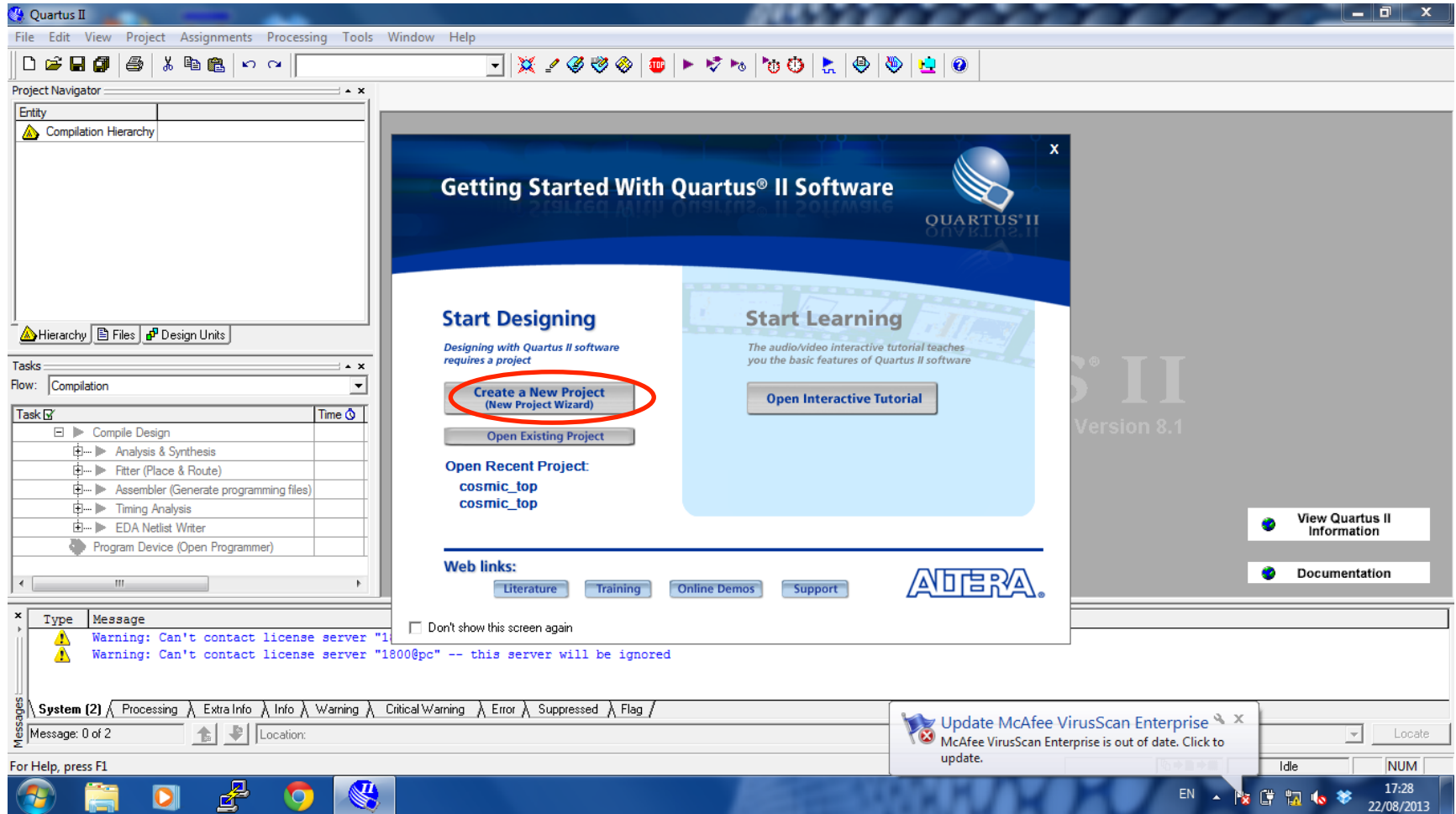
- *use external clock generator to drive the LEDs*

## You will write code in Verilog Hardware Description Language as well as use the schematic interface

- *No knowledge of Verilog is needed; the code will be provided and explained.*

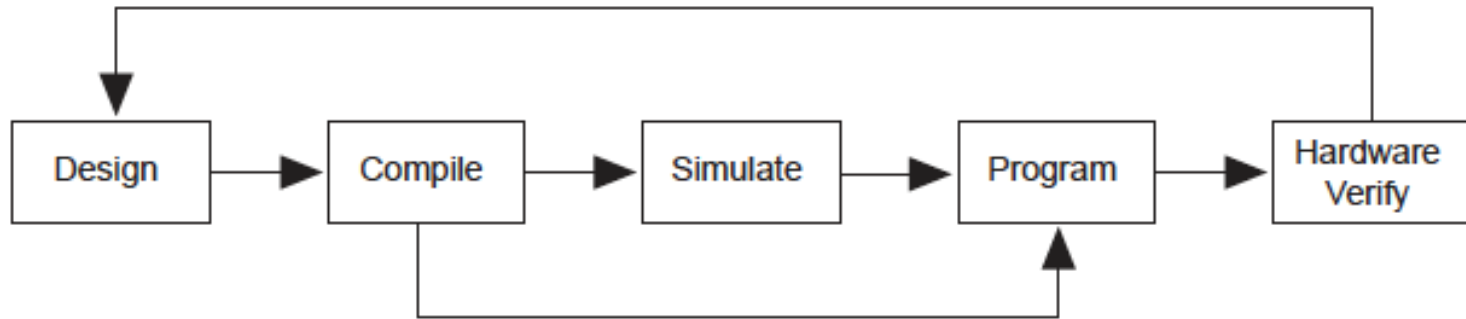
# The tutorial in 5 slides

- You will receive the full tutorial at the lab session
- Launch Quartus II:



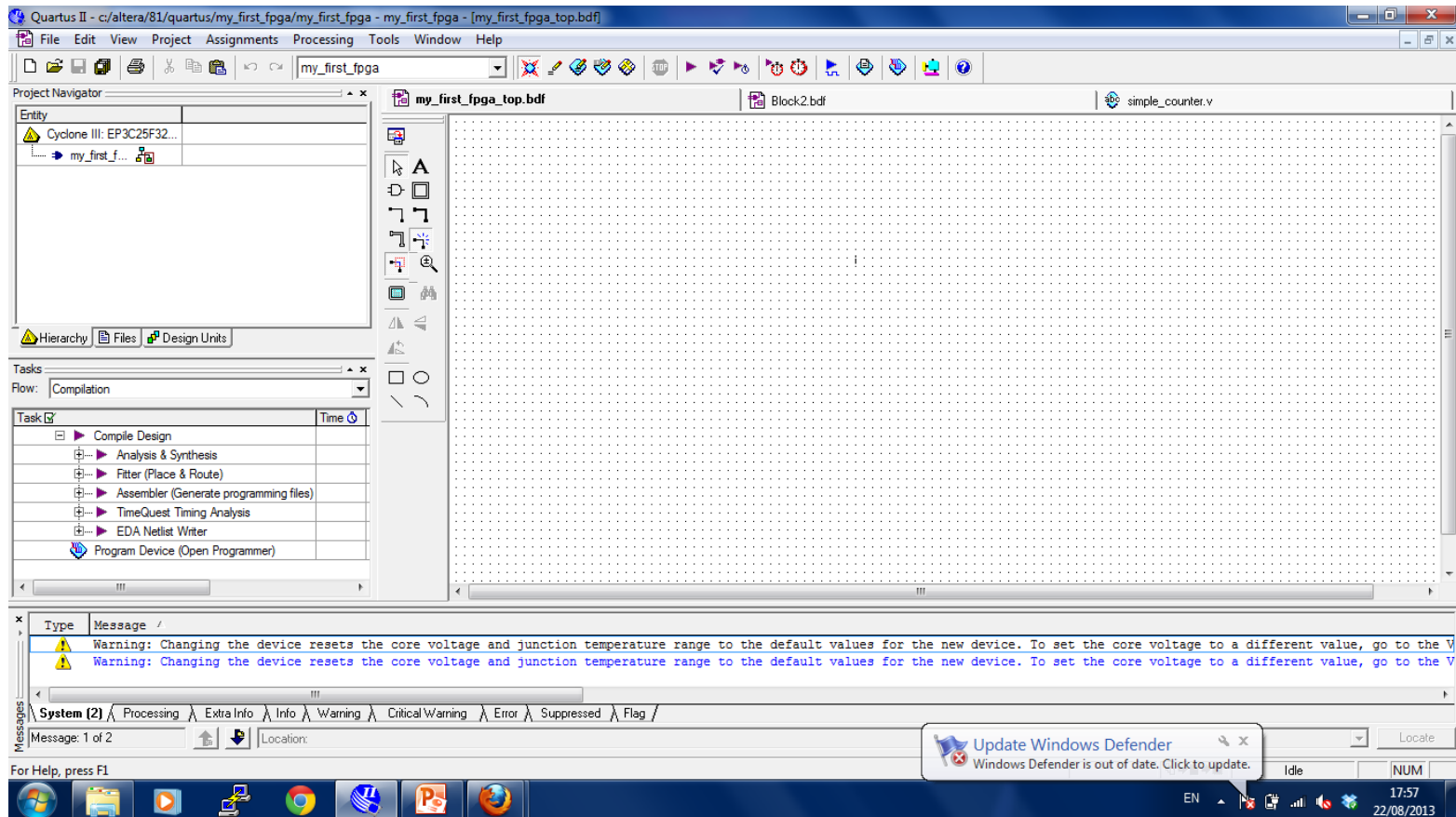
# The tutorial in 5 slides

- The design flow:



# The tutorial in 5 slides

- The design should match the hardware !
- The development board is equipped with a Cyclone III FPGA
  - *Name: EP3C25F324C6*
- Empty working area:



# The tutorial in 5 slides

- Write a first Verilog code to create a counter

The screenshot displays the Quartus II software interface. The main window shows a Verilog code editor with the following code:

```
1 //This is an example of a simple 32 bit up-counter called simple_counter.v
2 // It has a single clock input and a 32-bit output port
3 module simple_counter (input clock , output reg [31:0] counter_out);
4 always @ (posedge clock)// on positive clock edge
5 begin
6 counter_out <= #1 counter_out + 1;// increment counter
7 end
8 endmodule// end of module counter
```

The interface includes a Project Navigator on the left, a Tasks panel, and a Messages window at the bottom. The Messages window shows two warnings: "Warning: Changing the device resets the core voltage and junction temperature range to the default values for the new device. To set the core voltage to a different value, go to the V...". The Windows taskbar at the bottom shows the system tray with the date 22/08/2013 and time 17:58.

# The tutorial in 5 slides

Make from this counter a schematic object:

The screenshot displays the Quartus II software interface. The main workspace shows a schematic diagram of a component named 'simple\_counter'. The component is represented by a rectangular box with a blue border. Inside the box, the text 'clock counter\_out[31..0]' is visible. The component is labeled 'inst' at the bottom left corner. The interface includes a Project Navigator on the left, a Tasks pane, and a Messages pane at the bottom. The Messages pane shows the following text:

```
Info: Running Quartus II Create Symbol File
Info: Command: quartus_map --read_settings_files=on --write_settings_files=off my_first_fpga -c my_first_fpga --generate_symbol=C:\altera\81\quartus\my_first_fpga\simple_counter.
Info: Quartus II Create Symbol File was successful. 0 errors, 1 warning
```

The Windows taskbar at the bottom shows the system tray with the date 22/08/2013 and time 18:00. A notification bubble for McAfee VirusScan Enterprise is also visible.

# The tutorial in 5 slides

After some steps:

The screenshot shows the Quartus II IDE with a logic design for a simple counter. The design includes a PLL block (inst1) receiving an OSC\_CLK input and outputting a clock signal (c0) to a simple\_counter block (inst). The simple\_counter block outputs a counter value (counter\_out[31..0]). This counter value is connected to a counter\_bus\_mux block (inst2), which also receives a button[0] input. The mux outputs a result[3..0] signal to an LED (led[3..0]).

The status bar shows "Processing (6)" and the message window displays information about running the Quartus II Create Symbol File command.

```
Info: *****
Info: Running Quartus II Create Symbol File
Info: Command: quartus_map --read_settings_files=on --write_settings_files=off my_first_fpga -c my_first_fpga_top --generate_symbol=D:\altera\my_first_
Info: Quartus II Create Symbol File was successful. 0 errors, 2 warnings
```



# The tutorial in 5 slides

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## ● Last steps:

- *Assign the pins (to effectively connect in the hardware the FPGA to the other devices – clock, button, GPIOs, etc.)*
- *Compile the your project*
- *Program the FPGA (through the USB interface)*
- *Run the program in FPGA hardware*

# References & practical infos

## ● ALTERA

- <http://www.altera.com/>

## ● My First FPGA Design

- [http://www.altera.com.cn/literature/tt/tt\\_my\\_first\\_fpga.pdf](http://www.altera.com.cn/literature/tt/tt_my_first_fpga.pdf)

## ● The Design Warrior's Guide to FPGAs: Devices, Tools and Flows

- *C. Maxfield, ISBN 0750676043*

## ● Note : we could have done the same with Xilinx FPGAs ;-)

- <http://www.xilinx.com/>

## ● For the lab sessions:

- *Each group of students will have 1 FPGA board, 1 oscillo and notes*
- *We have Windows laptops, but you could also do it on your laptop*
  - Install before the lab **quartus II web edition**

<http://www.altera.com/products/software/quartus-ii/web-edition/qts-we-index.html>