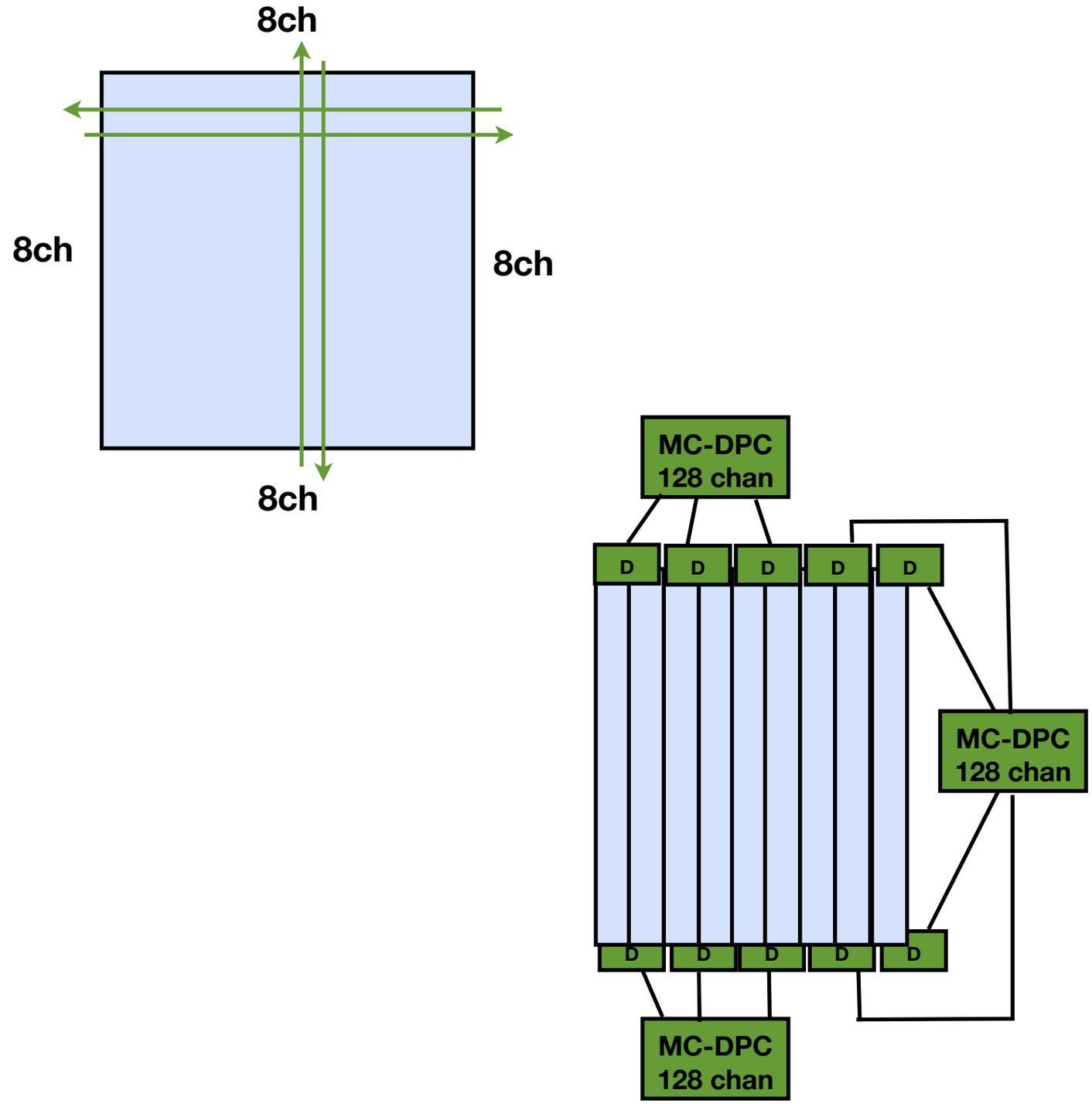
# SoLid electronics status

# Key Features

- Signal from MPPC : 65 MHz in 14bit 16chan ADC
- 64 to 128 channel read out per board
- FPGA on board processing
    - zero suppression, readout thresholds, DPP for neutron trigger
- MPPC bias voltage supply & individual voltage trims
- charge injection system for ADC linearity and checks
- temperature sensors
- Connectivity : Gigabit Ethernet, trigger in/out, clock in/out

# SM1 electronics Layout

- Plane has 4*8=32 channels
  - X and Y and flipped side
- Sub-module has 9x32 = 288 channels
- 10 DEIMOS boards
  - not all full so will need to arrange channel map to alleviate FPGA processing
- 3 DPC cards



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Notes DAC has two registers so that a square wave output can be setup independently on each output ?
DAC controlled via LDAC?

Could we use the dac to put test pulses onto the bottom of the mppc (have a resistor across the MPPC) and this could then reduce components even further. The resistor across mppc would increase dissipation though.

Output of trans-impedance amp vcc/2 +/-1v ? check

Add temp sensor

32x HV RCRCR filters

+75v?

+5v

+5v

32x MPPC connectors

32

32 channel Trans-impedance amplifier

32 x2

80 way connector emi smc male right angle socket

80 way connector emi smc female idc connector

80 way ribbon cable

80 way connector emi smc female idc connector

80 way connector emi smc male right angle socket

8

40th channel as monitor

0-31

32

32-39

40 channel DAC

SPI

LDAC

AVDD
+4V5 -5V5

DVDDio
+2V7 - 5V5
1mA

10KΩ
390pF
To GND

Can we set up voltage range so that we do not need a dac to control the hv side ?
Analog side of dac is powered by 5v and therefore should have a 5v range.

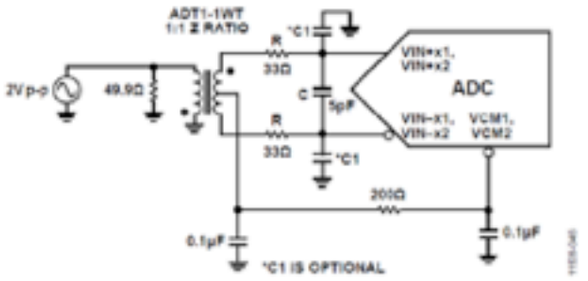



Figure 36. Differential Transformer Coupled Configuration for Baseband Applications

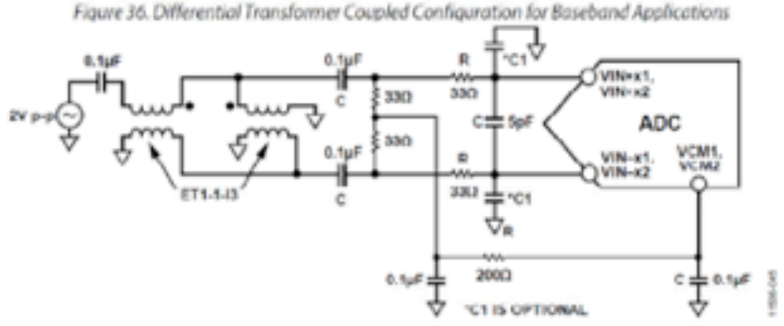



Figure 35. Differential Double Balun Input Configuration for Baseband Applications

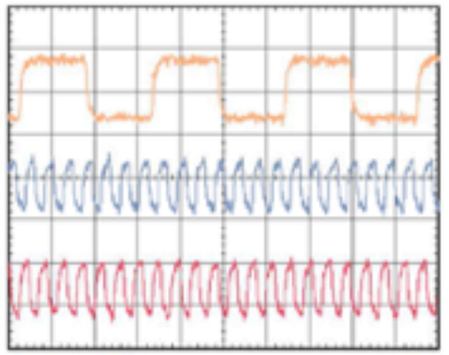



Figure 46. LVDS Output Timing Example in ANSI-644 Mode (Default)

5V0
Range 2v5 – 16v0

75V0

HV PSU

?

5V0

3V3 1mA

AVDD =+1V8

DRVDD =+1V8

32 channel Baluns or tranformers ?

32 x2

16 channel adc 14 bit 65 MHz

CM

16 channel adc 14 bit 65 MHz

CM

SPI

LDAC

32top, 32 bot

240 way

60 x4 way

Master clock system on board, using address scheme 00 is master.

FCO = 65MHz
DCO = 455 MHz (DDR)
DATA = 910 Mbps
All signals LVDS

Clk 455MHz (65x14/2)

FCO1,DCO1, D(A-H)1

sync

FCO2,DCO2, D(A-H)2

Clk 455MHz (65x14/2)

FCO1,DCO1, D(A-H)1

Sync ?

FCO2,DCO2, D(A-H)2

2

20

2

20

20

20

3V3 IO

3V3 IO

Us dual convertor, to sync convertors, 3v3 will be low current .
Do not need to input 5v, higher may be more efficient with smps.

3V3 SMPS
VCCIO
Range 0v8 – 3v6

5V0
Absolute max 7V0

1V8 SMPS
VCCIO
Range 0v8 – 3v6

1V0 (0V9)
SMPS
VCCINT
Range 0v8 – 3v6

System monitor ADC

1V8 IO
Unless stated

Kintex7
FPGA
XC7K325T

3V3

SFP+ Module in cage

Ethernet
10,100,1000
?

External clock input

LVDS Clock module

JTAG port

PROM

5V0
5V0
5V0

SATA power connector 15 pin

SATA serial data x2 connector 7 pin

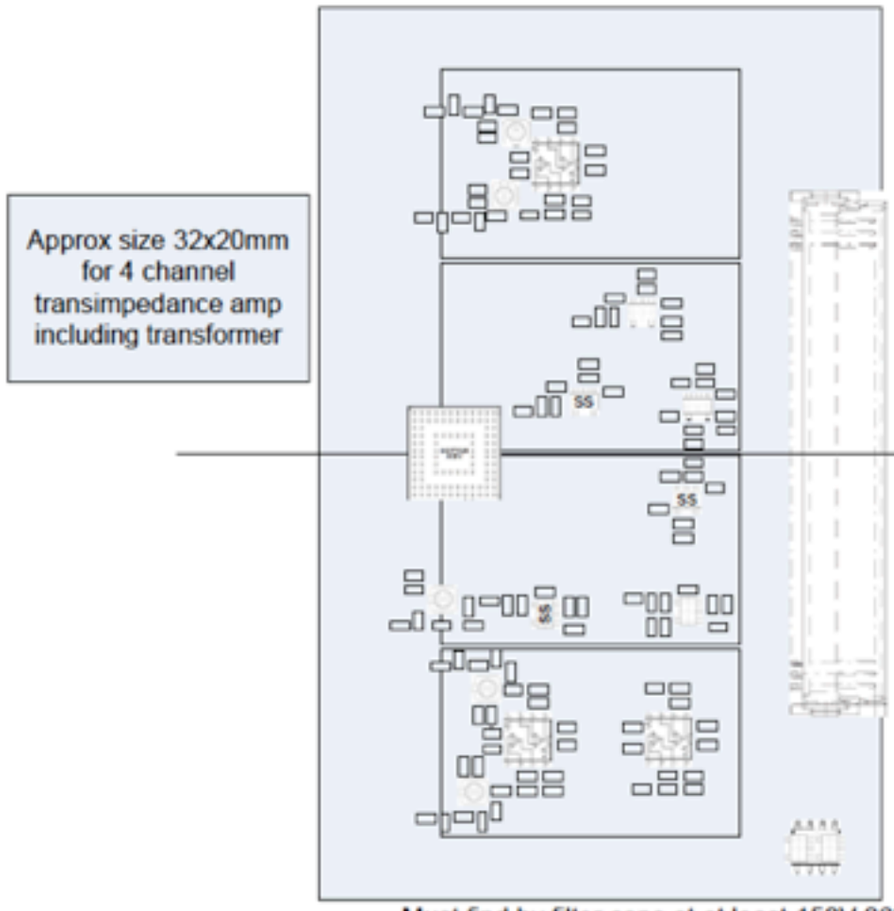
LVDS to neighbour

LVDS to neighbour

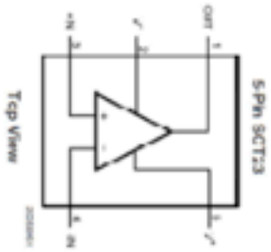
# DEIMOS front end board V2

Gnd side of mppc cables must not touch anything at either end since they are not actually gnd.

All voltages are feed through on single 80 way ribbon cable.
Transformer should be nest to the adc, but we can use gnd to produce pseudo diff signal.
Calibration done through top 8 channels of 40 channel DAC using LDAC.
No Cal voltage since cal is done using DAC.
HV switch is now on main board.



Approx size 32x20mm for 4 channel transimpedance amp including transformer



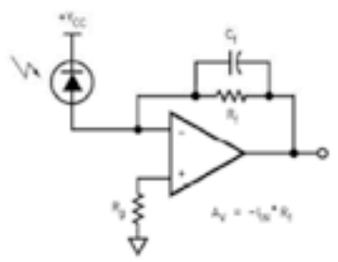



FIGURE 7. Transimpedance Amplifier Configuration

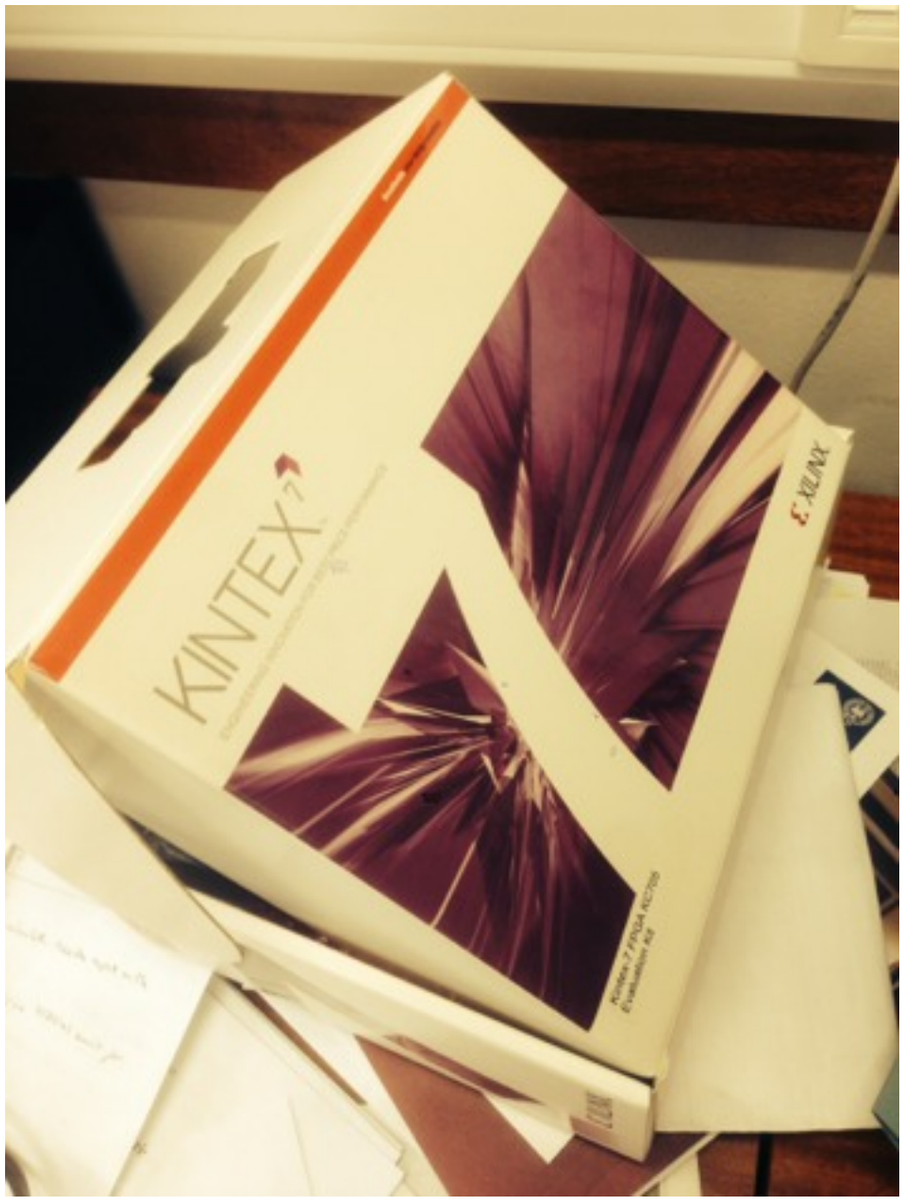
Must find hv filter caps at at least 150V 0603 biggest C.
KEMET - C0603C103K2RACTU - CAP, MLCC, X7R, 10NF, 200V, 0603

# Firmware

- will use interface developed at CERN (CACTUS) for CMS level-1 trigger
  - https://svnweb.cern.ch/trac/cactus
  - and some IPbus example firmware for Xilinx dev boards : https://svnweb.cern.ch/trac/cactus/browser/trunk/boards/ipbus_demo/projects/demo_kc705_basex
- ADC synchronisation : R. Wastie and A. Baird
- DAC and other functionalities : R. Wastie
- data processing and output : N. Ryder

# Kintec 7 dev board available

- Nick has borrowed ATLAS dev board to start developing
  - ordering one for SoLid this week



# Current status

- finalise footprint of DEIMOS card before end of month to feed in mechanical design

- finalise board design mid-may for first production (DPC and DEIMOS)

    - boards are simplified so no major issue are expected with layout and routing this time

    - will produce 2-3 DEIMOS board so we can fit one on the frames by end of may

- DPC firmware work will start in May